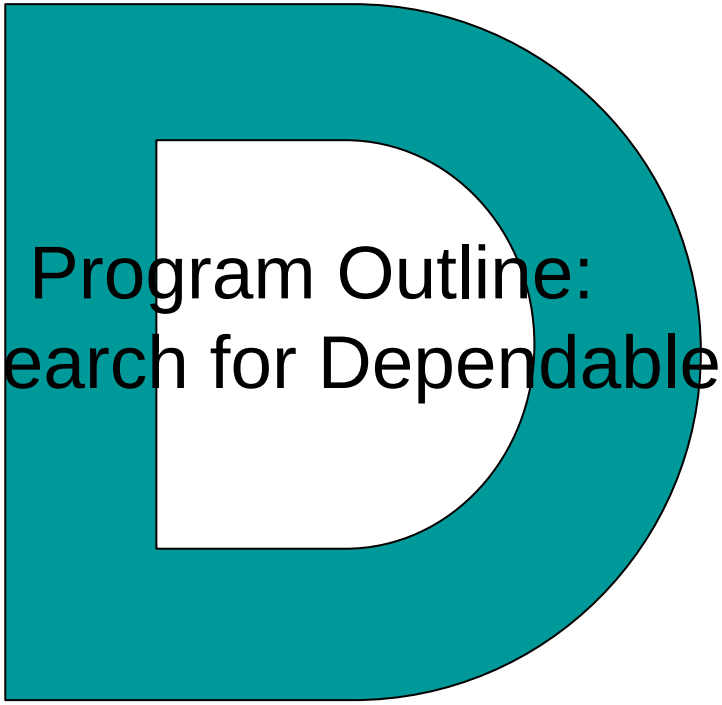
A Research Program Funded by Japan Science and Technology Agency during FY 2007-2014

Program Outline: Fundamental Research for Dependable VLSI Systems



May 16, 2012

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Rationale for research on DVLSI

VLSI: VSI is at the core of systems and its dependability underlies systems dependability.
Problems: Threats to dependability is actually increasing.

Threats arising from miniaturization

Variations in dimensions, shape, doping,
Reduction in signal/noise (radiation, EMI, fixed and floating charge),
Aggravating wear/fatigue phenomena

Threats from increased complexity

Enhanced functionality (identification, encryption,---)
Multiple- many-core architectures,
Heterogeneous integration; Analog, digital, nonvolatile, network, sensors, actuators, etc.

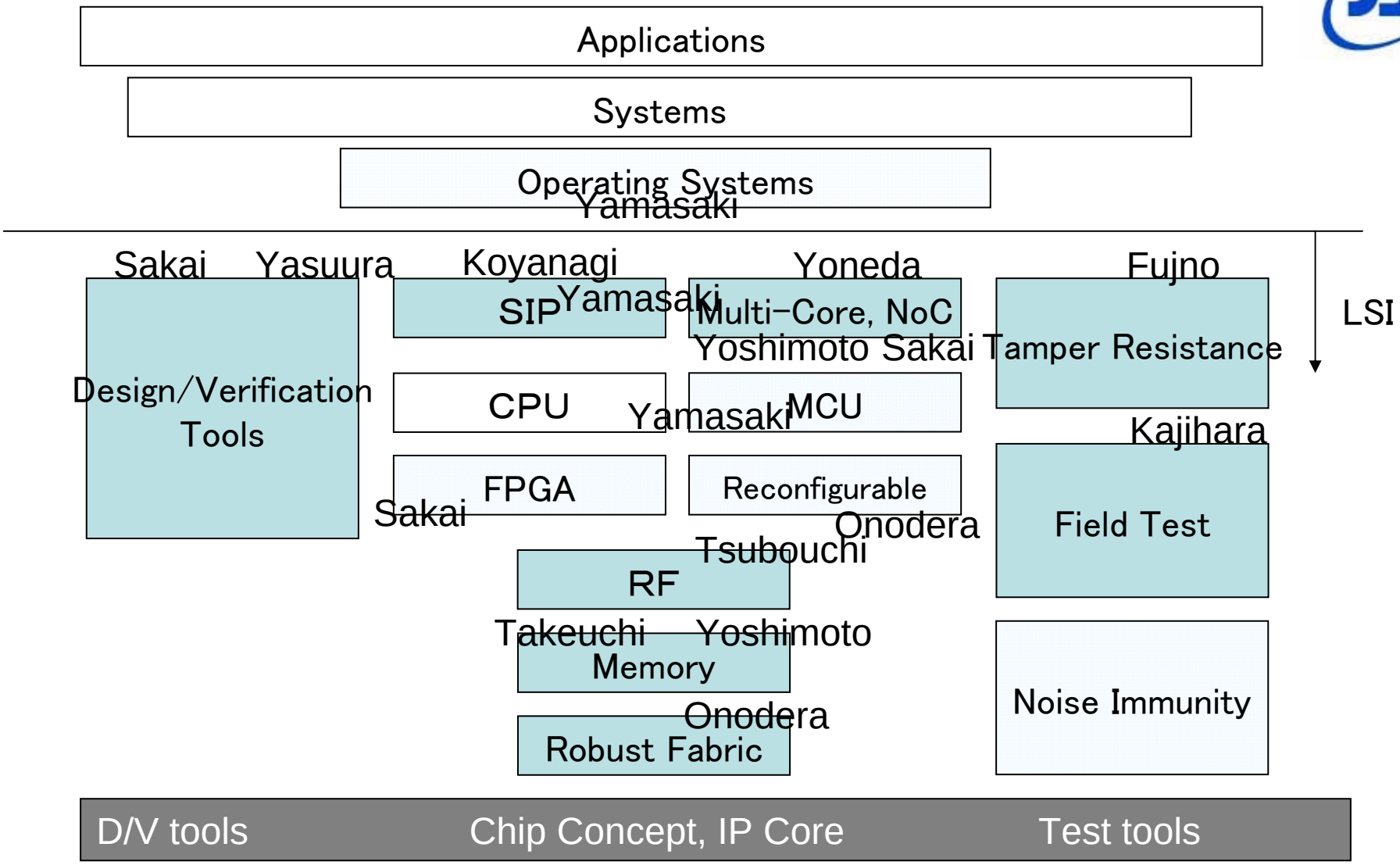
Our Mission at CREST/DVLSI

1. Contain Rising Threats within VLSI (Component Supposed to be Most Dependable)
2. Provide New Functionalities in VLSI Which Improve Dependability at the Systems Level

Projects and Principal Investigators

FY Started	PI	Affiliation	Project
2007	Hidetoshi Onodera	Kyoto University	Dependable VLSI platform using robust fabrics
	Shuichi Sakai	The University of Tokyo	Ultra Dependable VLSI by collaboration of formal verifications and architectural technologies
	Kazuo Tsubouchi	Tohoku University	Development of Dependable Wireless System and Device
	Hiroto Yasuura	Kyushu University	Modeling, Detection, Correction and Recovery Techniques for Unified Dependable Design
2008	Seiji Kajihara	The Kyushu Institute of Technology	Circuit and system mechanisms for high field reliability
	Masahiko Yoshimoto	Kobe University	Dependable SRAM Techniques for Highly Reliable VLSI System
	Tomohiro Yoneda	The National Institute of Informatics	Development of Dependable Network-on-Chip Platform
2009	Mitsumasa Koyanagi	Tohoku University	Three-Dimensional VLSI System with Self-Restoration Function
	Ken Takeuchi	Chuo University	Dependable Wireless Solid-State Drive (SSD)
	Takeshi Fujino	Ritsumeikan University	The Design and Evaluation Methodology of Dependable VLSI for Tamper Resistance
	Nobuyuki Yamazaki	Keio University	Fundamental Technology on Dependable SoC and SiP for Embedded Real-Time Systems

DVLSI Program covers:



Approaches taken and applications eyed