

# Circuit and System mechanism for high field reliability

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CREST/DVLSI

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# Background

- Aging of VLSI in field : sudden system down ... Safe & Secure
  - Aging phenomena: NBTI, HCI, Electro-migration, etc.
  - Increase of circuit delay ▪ ▪ ▪ difficult to expect the delay degradation
  - Worst case design or reliability-aware design : degradation margin considering process variation, operating conditions, expected life time ▪ ▪ ▪ excessive margin sacrifices performance.

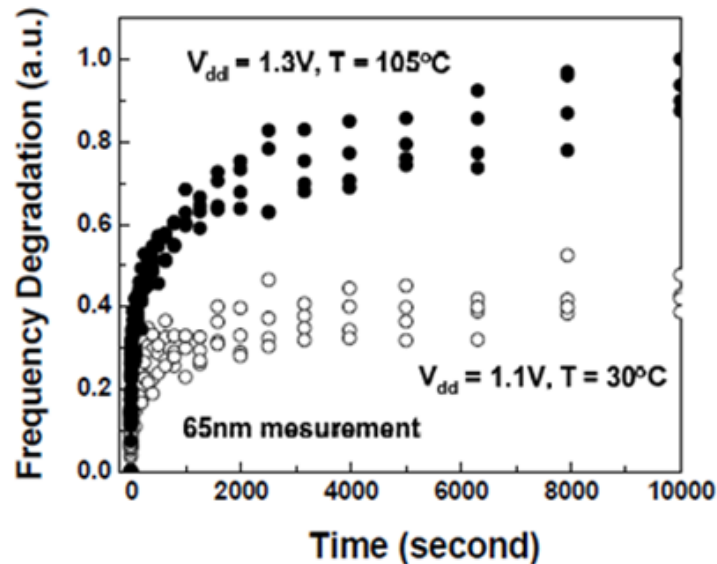


Fig. 1. Delay degradation by NBTI  
[Y. Cao(DRVW2008)]

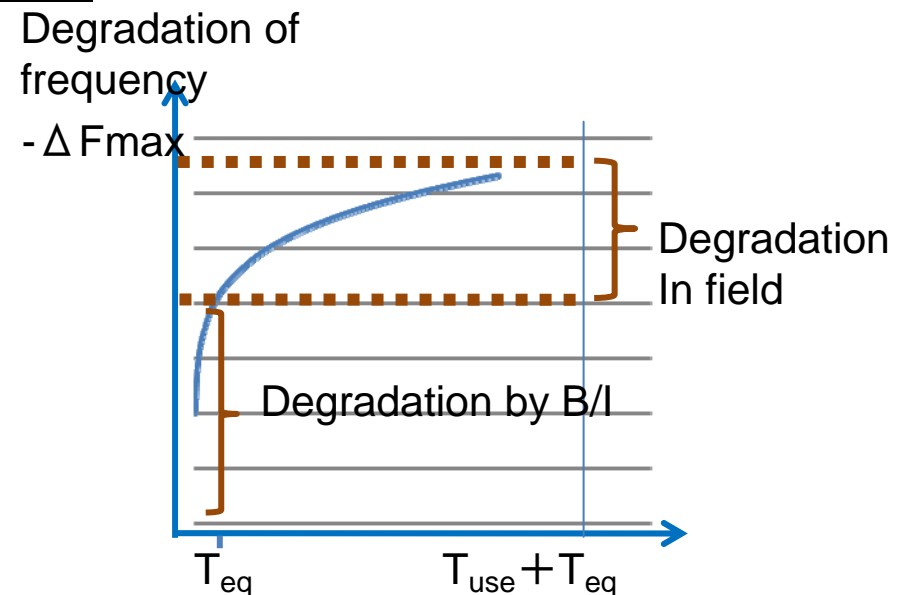


Fig. 2. Design considering degradation margin



# ***D·A·R·T Technologies***

Effective field test scheme to achieve high field reliability

DART : Dependable Architecture with Reliability Testing

- ***D :Degrade Factor***

- Predict degradation of SoC/NoC/FPGA

- ***A :Accuracy***

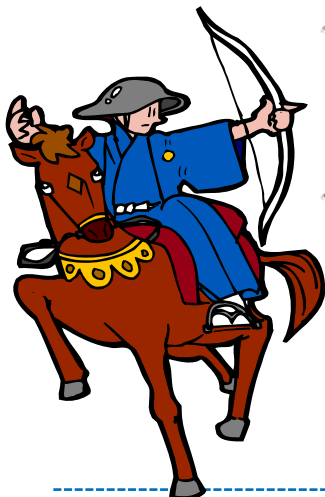
- Realize high detectability

- ***R :Report***

- Report failure information

- ***T :Test Coverage***

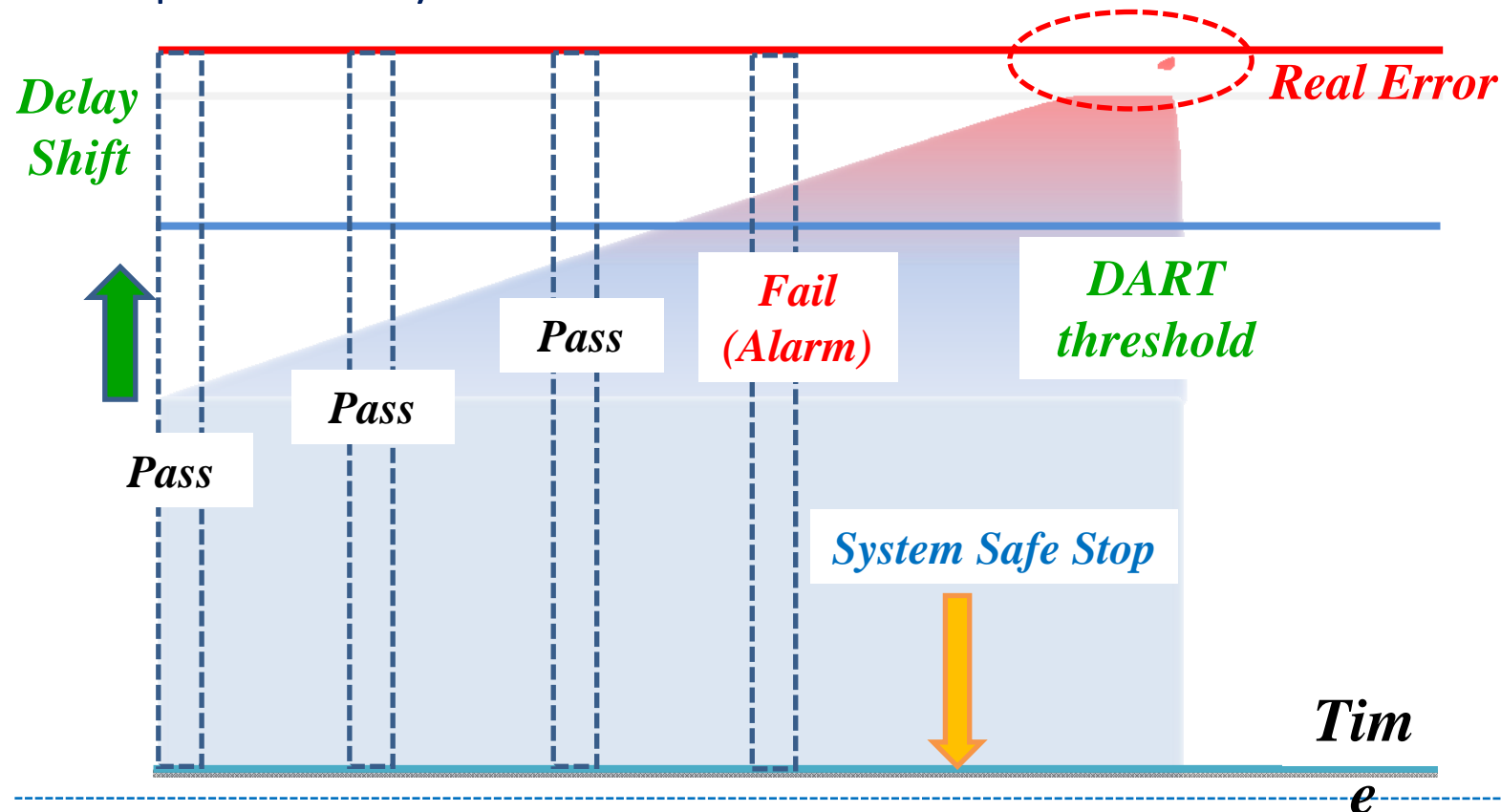
- Realize high test coverage





# Concept of Field Test by DART

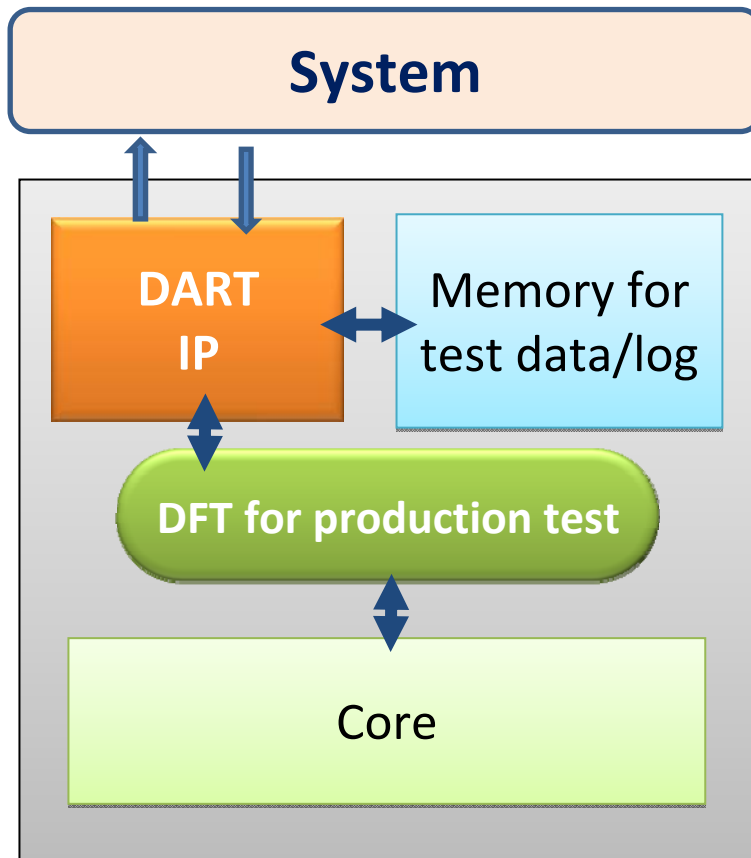
- Fault Detection and Identification of Aging by in-field test
- Measure path delay repeatedly in field at system idle/power-on mode and observe the decrease of delay margin.
- Report to the system and alert before a failure occurs.



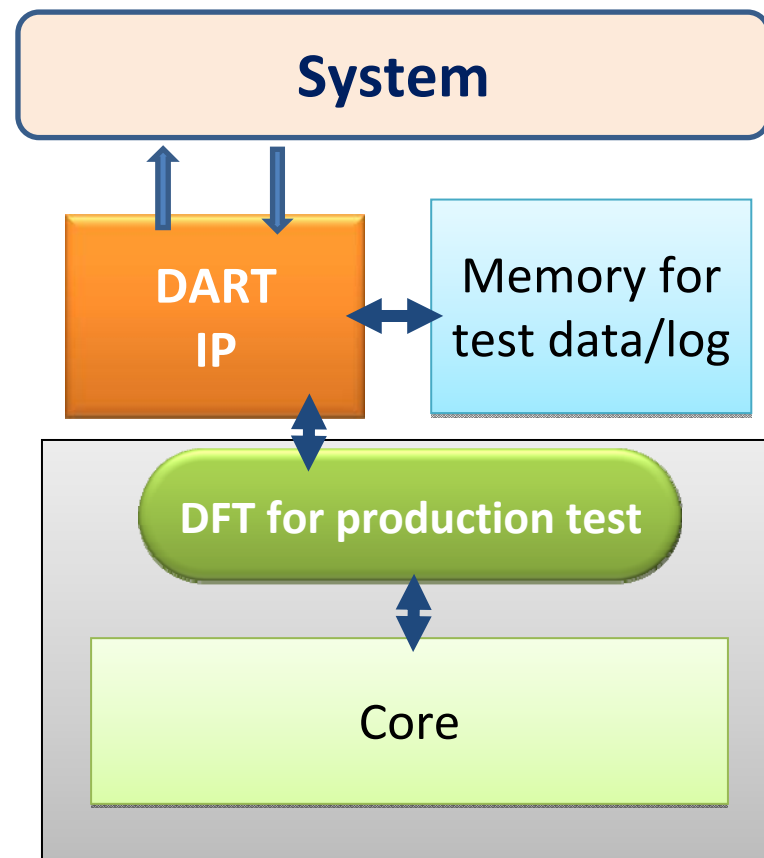


# DART architecture

- Control DFT for production test & logging test results



(a) On-chip DART



(b) Off-chip DART



# Comparison of Test Features

	Manufacturing Test	DART
Target	Fault (defect)	Delay Shift
Target (Status)	Static	Varying
Chance	One time	Repeated (in interval)
Method	Compare with threshold (pass / fail )	Delay measurement (with history)
DFT	Scan / BIST	BIST (with variable timing)
Resource	ATE (Large memory, Controllable test time)	On/off-chip memory for data, log
Environment	Well-controlled (In a test cell)	Non-controlled (user environment)



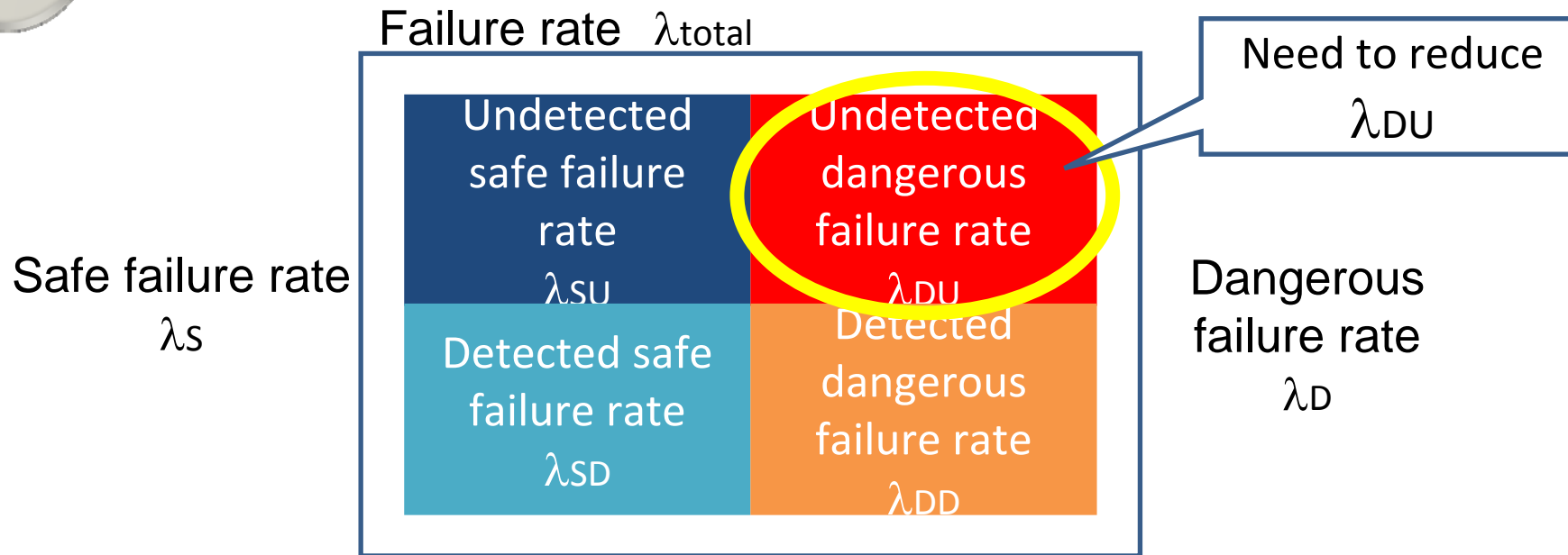
# Application Needs (Examples)

	Automobile, Medicine	Plants, Social infrastructure	Network, Storage, Server	Manufacturing Test
<b>Life Time</b>	Long ~20 years	Long 20~50 years	Medium ~10 years	—
<b>Field Test</b>	Power-on/off test	At assigned Test Mode	During Non-stop operation	—
<b>Test Resource (Memory etc.)</b>	Small LSI-pins & memory	Medium (Redundancy etc.)	Medium (Store some log)	rather Large (ATE)
<b>Test Time</b>	~10ms	~100ms	Dozens of 10~100ms	Few physical restrictions (low cost needed)

**Requirements are different from manufacturing test**



# Relation to IEC61508



- **Diagnostic coverage : DC(%) IEC61508-4 3.6.6**  
percentage of detected dangerous failure by DART for all dangerous failure

$$DC = \lambda_{DD} / (\lambda_{DD} + \lambda_{DU})$$

- **Safe failure fraction : SFF(%) IEC61508-4 3.6.15**  
 $SFF = (\sum \lambda_s + \sum \lambda_{DD}) / (\sum \lambda_s + \sum \lambda_{DD} + \sum \lambda_{DU})$



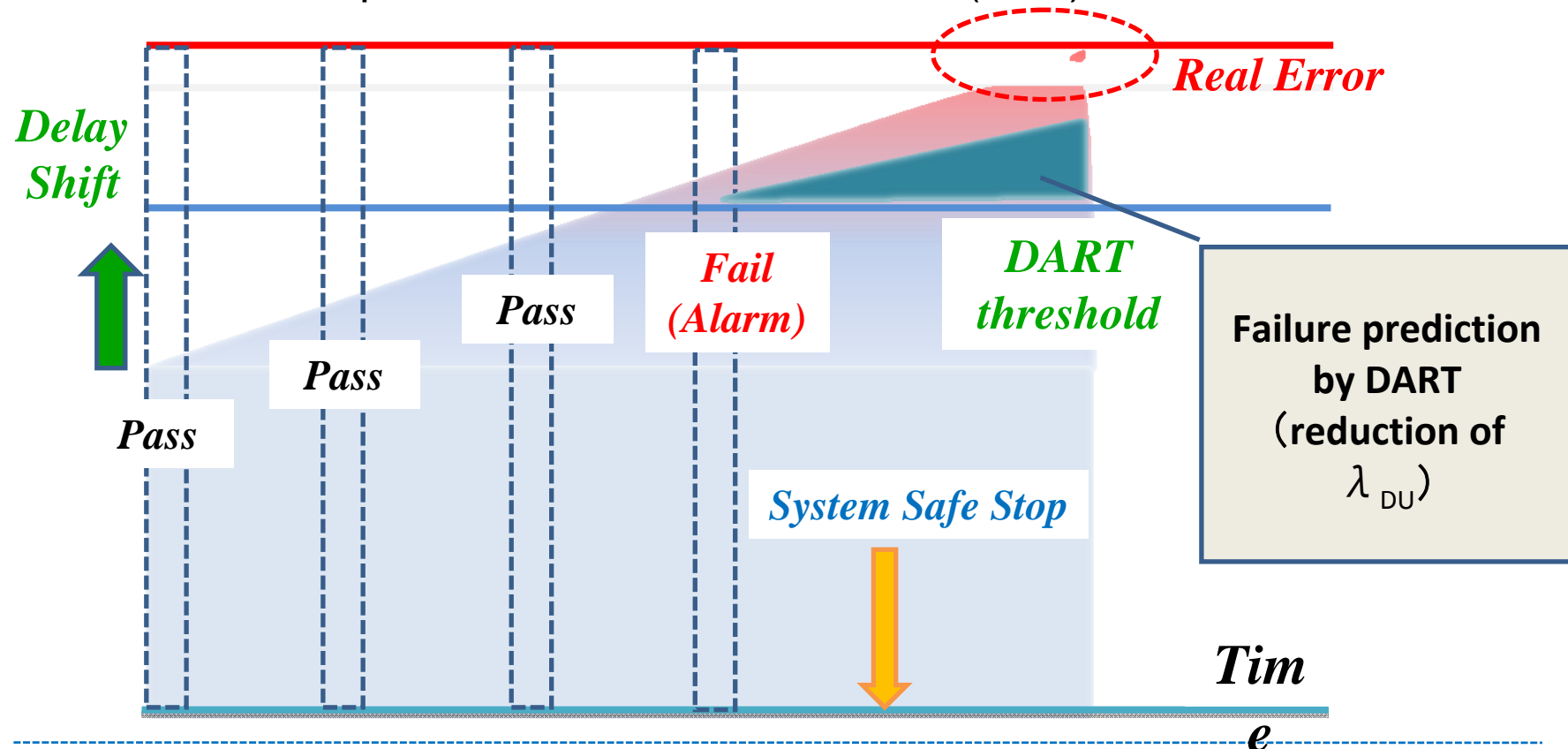


# Effects of Field Test by DART

■ DART changes undetected dangerous failure ( $\lambda_{DU}$ ) to detected dangerous failure ( $\lambda_{DD}$ )

$$\lambda_D \rightarrow \lambda_D \times (1 - DC) \quad DC: \text{Diagnostic Coverage of DART}$$

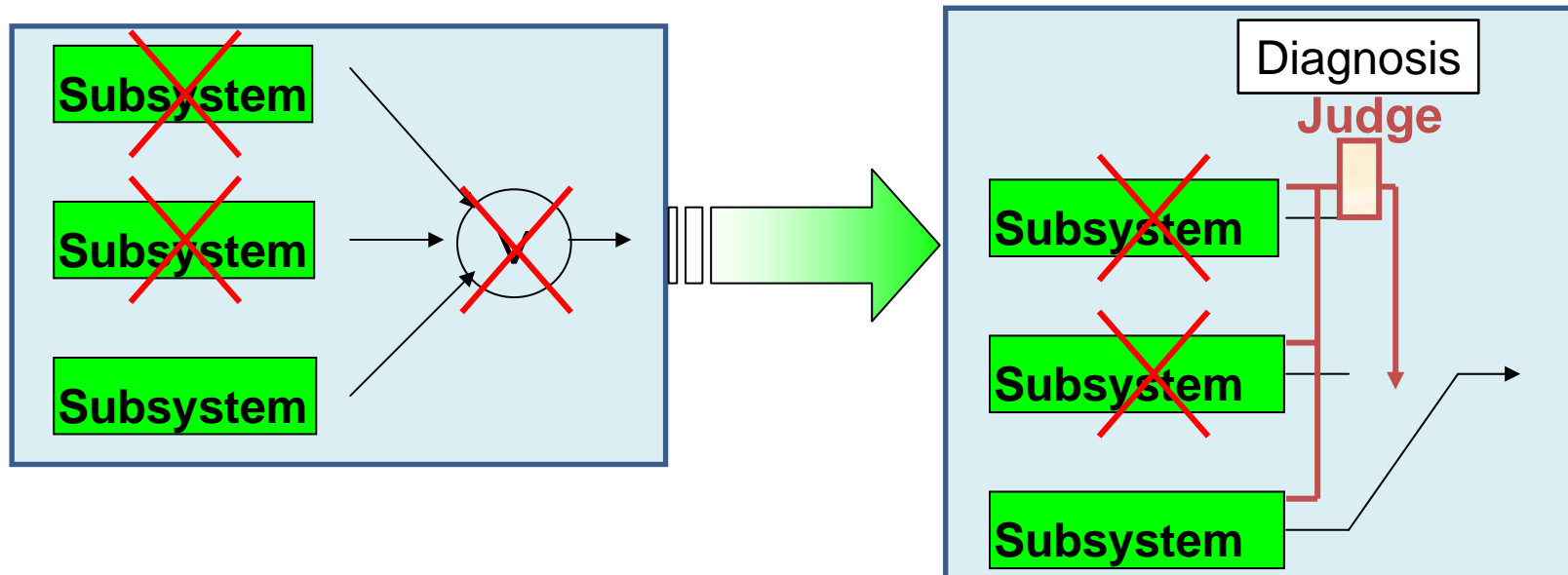
■ DART improves Safe Failure Fraction (SFF).





# Conclusions

- DART: A new field test scheme for failure prediction
  - Measure delay degradation and alert before a failure occurs.
- IEC61508: Reduction of Undetected dangerous failure rate
  - Avoid Common Cause Failure in redundant system (NMR)



- Provide high diagnostic coverage especially for a safety-related system.