Circuit and System Mechanisms  
for  
High Field Reliability  

- DART Technology -  
(Dependable Architecture with Reliability Testing)  

White Paper  
Version 4.1  
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1. Introduction

This white paper describes the outline of DART technology [1, 6, 15] undergoing as a part of research activities on "Fundamental Technologies for Dependable VLSI Systems," which is one of research areas of Core Research for Evolutional Science & Technology (CREST) by Japan Science and Technology Agency (JST).

1.1 Background

Advances in semiconductor process technology have brought up various aging issues in field operation of LSIs. There are many aging mechanisms, such as, BTI (Bias Temperature Instability), HCI (Hot Carrier Injection), TDDB (Time Dependent Dielectric Breakdown), EM (Electromigration) and SM (Stressmigration). Fig. 1-1 shows an example of real measurement data of frequency degradation by NBTI (Negative BTI). From this figure, it is clear that the delay increase caused by NBTI results in frequency degradation over time. It is, however, noted that the amount of delay increase is hard to estimate accurately since it depends on environmental parameters, such as temperature and voltage, and operating status, such as PMOS active ratio.

In order to avoid system failure caused by aging, recent designs usually set a certain amount of margin on operational frequency. However, some applications may require very large, say 5-15%, margin since it is determined based on the worst case condition of process variations, operational environment, expected lifetime, and so on. In such cases, LSI performance will be sacrificed. Fig. 1-2 shows an example of frequency degradation caused by NBTI, which requires reliability-aware design with large margin. As shown in Fig. 1-2, the amount of frequency degradation is estimated by the evaluation of TEG (Test Element Group) where the amount of degradation by burn-in (B/I) and in field should be also taken into account, and so the reliability-aware design leads to a large degradation of operational frequency.

The utilization of online testing to monitor circuit outputs and internal signals in operation is often used as another solution to avoid system failure. There are several well-known methods, such as, parity checking, and stability checking using dedicated flip-flop, for monitoring soft errors, noises and other temporary failures. However, the dedicated flip-flop needs large area overhead, that is, its area is more than the triple of ordinary flip-flop, and so, it can be used only for a part of flip-flops. As a result, it is difficult to guarantee the field reliability of the whole circuit by the utilization of such flip-flops. Moreover, these monitoring methods may need a lot of time to repair, since they detect faults only after some abnormal outputs are observed in operation.

In order to overcome these issues, high level reliability assurance, such as an exhaustive test of whole circuit, the detection of aging progression and the prediction of system failure, and so on, should be realized.

- You can improve in-field dependability of your system.
- LSI may degrade even if it is properly manufactured.
  
  Delay margin degradation by aging increases the risk of malfunction due to noises.
  
  Sudden system down can be avoided by advance detection of failures caused by aging.
- You can improve system dependability in low cost, since your manufacturing test framework is reused.
- You can also improve system debug efficiency and manufacturing test quality.
- Binning of highly reliable chip can be realized, since delay margin is measured before shipping.
- In-field system debug efficiency can be improved, since on-chip information is observed.
- You can improve quality in low cost, since delay test quality can be optimized under test time constraint.

**DART technology can support security and safety of your system.**

---

![Fig. 1-1 Frequency Degradation by NBTI](image1)

(c.f. Y. Cao, DRVW2008)

![Fig. 1-2 Reliability-Aware Design](image2)

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DART White Paper (Version 4.1)
1.2 Objectives

The target of the field test technology proposed in this research is the assurance of high level reliability by quick and high quality test for a shipped LSI, or a part of the shipped LSI, in test mode. As shown in Table 1-1, in field test, there are various test constraints, such as operational environment, test data volume, test application time, and so on, depending on its application. For example, the operation period of network servers is less than 10 years while that of plant control or social infrastructure systems is required to be as long as 30 years. The objective of the research is to develop elemental technologies corresponding to these constraints and also an integrated self-test technology to implement field testability function to application systems. Furthermore, the research also aims to contribute to the whole community by demonstrating the practical applicability of the DART technology to highly dependable systems through feasibility studies of developed technologies, and providing a guideline for realizing the DART technology on LSIs.

Table 1-1 Application Systems and Field Test Constraints

<table>
<thead>
<tr>
<th>Constraints</th>
<th>Automobile, Medical Systems</th>
<th>Plant Control Systems, Social Infrastructure, etc.</th>
<th>Network Server, etc.</th>
<th>Ordinary LSI Manufacturing Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operation Period</td>
<td>long (~20 years)</td>
<td>very long (~30 years)</td>
<td>medium (~10 years)</td>
<td>N.A.</td>
</tr>
<tr>
<td>Field Test Timing</td>
<td>power on</td>
<td>periodical test mode in operation</td>
<td>in operation (non-stop)</td>
<td>N.A.</td>
</tr>
<tr>
<td>Test Resource (memory size, etc.)</td>
<td>low pin count, small memory size</td>
<td>constrained (redundant design, etc.)</td>
<td>constrained (aging data memory, etc.)</td>
<td>a few constraints (on ATE)</td>
</tr>
<tr>
<td>Test Time</td>
<td>~10ms</td>
<td>~100ms (related to frequency)</td>
<td>50~500ms</td>
<td>physically few (some on cost)</td>
</tr>
</tbody>
</table>

2. Outline of DART Technology

2.1 What’s DART Technology

As an approach for field testability, we are developing a circuit and system architecture, called DART, for advance degradation detection and fault detection utilizing self-test and self-diagnosis of LSIs at system unoccupied time, such as power-on, power-off and idle time or dedicated maintenance time. For the DART technology, the following four targets are considered not only for elemental technology development but also for feasibility study and system integration.

D (Degradation Factor) : advance degradation detection of SoC/NoC/FPGA
A (Accuracy) : high accuracy detection
R (Report) : report of degradation information in field
T (Test Coverage) : realization of high test coverage

The basic concept of the DART technology is shown in Fig. 2-1. The DART technology calculates the amount of degradation of a chip by comparing measured delay with the initial value before shipment and issue an alarm to the system before the longest path delay of the chip exceeds allowable delay limit for prompting an action to avoid sudden system down. Thus we can reduce not only the failure rate of the system but also its repair time.

Fig. 2-1 Basic Concept of DART Technology
Fig. 2-2 shows the concept of the DART technology application. The DART technology requires a DART test controller for field test operation. The test controller for DART communicates with manufacturing test controllers, such as logic BIST (Built-In Self-Test) controller and memory BIST controller, to realize field test of each IP core on the chip. Test patterns for field test are stored in ROMs or non-volatile memories. The logs of field test results are also stored in non-volatile memories. The DART test controller and these memories can be located on-chip or off-chip. Though the test operation for each core is controlled by a certain core test controller, the DART test controller specifies the test timing based on the information obtained from temperature and voltage (TV) monito for accurate detection of the degradation of circuits in the core.

The DART technology has a good possibility to enhance functional safety of a system. Table 2-1 shows the range of detectable failures by DART and other existing approaches. It is noted that system multiplication, approaches, such as duplication, majority voting, and so on, can provide very high detectability for most failures, but they are hard to detect common cause failures (CCFs) brought by aging. It is also noted that existing approaches can provide only posteriori detection, that is, they cannot detect failures caused by degradation in advance of real failures, while DART has a capability of advance detection of degradation appearing as delay increase.

![Fig. 2-2 Image of DART Technology Application](image)

Table 2-1 Range of Detectable Failures by DART

<table>
<thead>
<tr>
<th>Cause of Failure</th>
<th>Appearance</th>
<th>System Multiplication (*1, 2)</th>
<th>On-Line Test (monitor, etc.) (*2)</th>
<th>In-Field BIST (*2)</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stuck fault</td>
<td>sudden stuck (random)</td>
<td>very high</td>
<td>low ~ medium (inexhaustive)</td>
<td>very high</td>
<td>very high</td>
</tr>
<tr>
<td>EM / SM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HCI / NBTI / PBTI</td>
<td>gradual delay increase (systematic)</td>
<td>low ~ medium (CCF)</td>
<td>low ~ medium (inexhaustive)</td>
<td>very high (posteriori)</td>
<td>very high (in advance (*3))</td>
</tr>
<tr>
<td>TDBB</td>
<td>delay increase → gate open (random)</td>
<td>very high</td>
<td>low ~ medium (inexhaustive)</td>
<td>very high (posteriori)</td>
<td>medium ~ high (in advance (*3))</td>
</tr>
<tr>
<td>Noise</td>
<td>marginal (temporary)</td>
<td>very high</td>
<td>low ~ medium (inexhaustive)</td>
<td>low</td>
<td>medium ~ high (in advance (*3))</td>
</tr>
<tr>
<td>Soft error</td>
<td>temporary (nonrecurring)</td>
<td>very high</td>
<td>low ~ medium (inexhaustive)</td>
<td>low</td>
<td>low</td>
</tr>
</tbody>
</table>

*1: hard to detect common cause failures (CCFs)
*2: only posteriori detection
*3: DART only feature
Fig. 2-3 shows an example of product development flow to implement the DART technology to a system. Following this flow, system reliability can be enhanced by implementation of the DART technology on LSIs in system design and LSI design phases and utilizing the implemented DART technology for field test phase.

2.2 Research Targets

Based on the DART technology given in the previous section, we define four issues for establishing the DART technology and breakdown the issues to research targets as shown in Table 2-2.

The first issue is accurate delay measurement, which requires to measure circuit delay accurately in field. The DART technology utilizes self-test and self-diagnosis to measure path delays in the circuit and predicts or detects the occurrence of fault due to aging. It realizes delay measurement in an accuracy one or two order finer than system clock cycle, then judges the level of degradation from the increase of measured delays, and predict the occurrence of system failure due to aging in advance.

The second issue is test constraints consideration, which requires the satisfaction of dedicated constraints on test time, test data volume and so on, for each application system. Though the target values shown in Table 2.2 are very severe comparing with those for manufacturing test, the DART technology can reduce the impact of its implementation on the system by establishing these targets.

<table>
<thead>
<tr>
<th>No.</th>
<th>Issue</th>
<th>Target Specification</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Accurate delay measurement</td>
<td>delay measurement error ≤ 50ps (for 300-500MHz circuits)</td>
<td>digital measurement of temperature and voltage variation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>temperature variation ≤ 5°C</td>
<td>to reduce error due to temperature variation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>fault coverage ≥ 95%</td>
<td>to ensure test quality</td>
</tr>
<tr>
<td></td>
<td></td>
<td>test data volume ≤ 1/3000</td>
<td>to embed in on-chip memory</td>
</tr>
<tr>
<td></td>
<td></td>
<td>test time per chance: 10-200ms</td>
<td>to avoid impact on system performance</td>
</tr>
<tr>
<td>2</td>
<td>Test constraints consideration</td>
<td>logic BIST based implementation</td>
<td>to reduce area overhead by utilizing existing test circuits and to reduce test data volume and power</td>
</tr>
<tr>
<td></td>
<td></td>
<td>asynchronous circuit support</td>
<td>to apply to NoC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>test record utilization</td>
<td>to enhance degradation detectability and diagnosis efficiency</td>
</tr>
<tr>
<td>3</td>
<td>Efficient implementation</td>
<td>guideline for DART implementation</td>
<td>to promote wide evaluation and implementation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>feasibility study for effectiveness validation</td>
<td>to validate practical applicability on performance, accuracy, field data acquisition and performance / environment monitoring in operation, by real chip, TEG or simulation</td>
</tr>
<tr>
<td></td>
<td></td>
<td>standardization for functional safety</td>
<td>to propose to add DART technology to conditions for IEC61508 SIL</td>
</tr>
</tbody>
</table>
The third issue is efficient implementation, which requires realization of in-field test functionality. Obviously, the implementation of the DART technology becomes more attractive by establishing these targets.

The fourth issue is practical application of the DART technology, which requires a guideline for DART implementation, called DART Implementation Guideline, to promote evaluation and implementation of the DART technology in wide range of potential application systems. Figure 2-4 shows the image of DART implementation workflow. DART Implementation Guideline, defining DART implementation works at each LSI design phase, can make it easy to implement the DART technology on LSIs. Moreover, the effectiveness of the DART technology on system dependability can be illustrated by validating the capability of efficient data acquisition and analysis of internal circuit delays by field test of DART implemented LSIs.

2.3 Approach for DART R&D

Several technologies for advance detection of degradation and failure detection utilizing in-field LSI self-test are developed as elemental DART technologies. Four research items shown in Table 2.2 are broken down into target requirements and elemental technologies covering these target requirements as shown in Fig. 2-5 are developed.
For accurate delay measurement, a statistical approach is used to reduce quantization error. In this research, a circuit delay is measured by LSI self-test in field, however, the circuit delay depends not only on degradation by aging but also on environmental conditions such as circuit voltage, temperature variation, and so on. Therefore, we are developing technologies for delay value compensation using circuit monitoring using TV monitors [13] and test temperature stabilization by thermal uniformity test [3, 9].

For satisfying test constraints on test application time, test data volume, and so on, which may differ from application to application, we are developing three techniques, that is, rotating test, high quality delay test set generation and degradation detection test. The rotating test technique scatters test set for whole chip in multiple test chances to reduce test application time and test data volume for each test chance [8]. The high quality delay test set generation technique co-optimizes delay test quality and test cost under the test constraints [2, 5, 7, 10, 14, 18]. The degradation detection test technique narrows down the test target considering aging mechanism and optimizing test for the aging mechanism to reduce test application time and test data volume [4]. Furthermore, we are working for improving BIST technologies for manufacturing test to reduce test data volume or power consumption during test [11, 16, 17].

For system integration, DART realizes test architecture for in-field test utilizing existing DFT frameworks, such as scan, logic BIST, and so on, for manufacturing test and in cooperation with proposing monitor circuits, test logging function, and so on [12]. The reuse of manufacturing DFT frameworks makes it possible to achieve high test quality in low hardware overhead.

For practical application, we are reviewing the developed technologies from the viewpoints of generalization and standardization, and provide a guideline for realizing them as DART modules. Furthermore, as a feasibility study, we are going to show the DART technology can be practically applicable by implementing the DART technology in real systems in cooperation with some companies and illustrating the target delay measurement accuracy can be achieved in realistic hardware overhead, test application time and test data volume. The developed technologies which are not embedded in the real system, we will validate them by test chip or by simulation. Moreover, we are going to work for the acceptance of the DART technology as a requirement for international standard of functional safety, IEC61508, to show its advantage and effectiveness in a form which is easily recognized by users.

2.4 Advantages of DART Technology

The DART technology and its ideas have advantages on applicability, superiority and originality as shown below.

The DART technology can realize field test utilizing scan design, logic BIST and so on which are implemented for manufacturing test. Moreover, the DART technology can be used both for field on-line test during system operation and for off-line test during system development and system debug on system halt. At on-line test, it can contribute to enhance system reliability in field by detection of delay increase through periodical delay measurement. On the other hand, at off-line test, it can not only detect low reliability chip in advance by measuring delay margin and initial degradation amount of the chip, but also contribute to efficient system debug in field by reporting on-chip delay information. Furthermore, the DART technology can provide techniques for optimizing test quality under severe constraints of test application time and test data volume and test and DFT techniques for asynchronous circuits. These technologies are also used in manufacturing test, and so they can contribute to enhance the quality of LSI chips including synchronous circuits, asynchronous circuits and GALS (Globally Asynchronous Locally Synchronous) systems.

As shown in Table 2-3, the DART technology has a possibility to be used for many purposes both on-line and off-line.

Table 2-3 Target Usages of DART Technology

<table>
<thead>
<tr>
<th>Target Usage</th>
<th>Purpose</th>
<th>Functionality</th>
</tr>
</thead>
<tbody>
<tr>
<td>Field Test (On-Line Use)</td>
<td>Advance detection of system failure due to aging</td>
<td>Log data analysis for checking delay margin transition</td>
</tr>
<tr>
<td></td>
<td>Diagnosis report on erroneous behavior</td>
<td>Report on tested paths and their delay margin</td>
</tr>
<tr>
<td>System Debug (Off-Line Use)</td>
<td>Monitoring of design margin and level of degradation</td>
<td>Acquisition of data on time passage, environmental effects, ordinary aging, accelerated aging, etc.</td>
</tr>
<tr>
<td></td>
<td>System diagnosis report</td>
<td>Report on delay information for failure analysis</td>
</tr>
<tr>
<td>Manufacturing Test (Off-Line Use)</td>
<td>Chip quality improvement</td>
<td>Maximization of delay test quality under test constraints Testability enhancement for asynchronous circuits</td>
</tr>
</tbody>
</table>
The adoption of the DART technology may largely depend rather on cost acceptability than on technical applicability considering the target usages. The DART technology is mostly suitable for plant control systems and social infrastructure systems among the application systems shown in Table 1-1, where redundancy is required for assuring long-term reliability. Moreover, it is suitable for network devices and servers where performance binning is necessary. On the other hand, for automotive LSIs and consumer LSIs, which have severe cost constraints on LSI pins and silicon areas, it is difficult to use the DART technology in current products, but we think it will be a necessary technology for next generation and beyond.

The DART technology has the following advantages comparing with similar researches.

- It can be applied to various types of LSIs including SoCs, NoCs and multicore.
- It can be also applied to FPGA-based systems.
- It can utilize the same DFT framework as used for manufacturing test, and so its impact to system can be minimized and it can even contribute to the efficiency of manufacturing test and system debug.

The DART technology has high novelty on the following points.

- Highly accurate measurement of delay margin of logic circuits by;
  - compensation functionality of measured delay value by monitoring the temperature and voltage during the delay measurement
  - aging-tolerant ring oscillators using standard cell library
  - simultaneous control of test power and temperature
- Flexibly adaptation to test constraints on test application time and test data volume by;
  - utilization of multiple test chances in field
  - effective test target selection
- Recording functionality of measurement logs and the capability of its application to system diagnosis

3. Outlines of DART Elemental Technologies

This section describes the outlines of some of DART elemental technologies, that is, temperature and voltage monitor (TV monitor), thermal-uniformity-aware test, partitioned rotating test, high quality delay test and low power BIST. Also some of our activities on DART implementation are shown.

3.1 TV Monitor

The DART technology uses temperature and voltage monitor to compensate environmental impact on circuit delay for accurate measurement. As shown in Fig. 3-1, temperature and voltage during test is estimated from the difference between initial and current count values of three ring oscillators (ROs), and then measured maximum frequency is compensated by the estimated temperature and voltage. It is noted that we can use aging-tolerant ROs [13] to avoid incorrect estimation.

\[
\begin{bmatrix}
T_e \\
F_e
\end{bmatrix} = \begin{bmatrix} a_1 & b_1 \\ a_2 & b_2 \end{bmatrix} \begin{bmatrix} k_1 F_{d1} - k_1 F_{d2} \\ k_1 F_{d2} - k_1 F_{d3} \end{bmatrix} + \begin{bmatrix} c_1 \\ c_2 \end{bmatrix},
\]

\[
F_e(T, V) = F(T, V) - F(T_e, V_e)
\]

Fig. 3-1 High Precision Delay Measurement by T-V Monitor

3.2 Thermal-Uniformity-Aware Test

The DART technology provides thermal-uniformity-aware test method to reduce temperature variation in time and space during in-field testing. A dedicated X-filling method is used for spatial uniformity as shown in Fig. 3-2 [3], and a dedicated pattern ordering method is used for temporal uniformity as shown in Fig. 3-3 [9]. The techniques realize small thermal variation during test, which will result in small delay variation (c.f. Fig. 3-4).

Fig. 3-2 Thermal-Uniformity-Aware X-Filling  Fig. 3-3 Thermal-Uniformity-Aware Pattern Reordering
3.3 Partitioned Rotating Test

The DART technology uses partitioned rotating test, which divides the whole test set into several test subset and use each test subset in a test chance by rotation as shown in Fig. 3-5, to satisfy test time constraint [8]. Adaptive change of test subsets can also be used to enhance degradation detection capability [12].

3.4 High Quality Delay Test

Many delay test generation approaches are developed in the DART technology to improve test quality for small delay defects. Figure 3-6 shows one of the approaches, which utilizes faster-than-at-speed test and achieves better SDQL (Statistical Delay Quality Level) in less test patterns [10].

Moreover, we propose a high speed per cell IR-drop analysis method as shown in Figure 3-7 [14, 18]. This enables an at-speed test taking account of the impact of IR-drop caused by power consumption during test, and contributes to high delay test quality.
3.5 Low Power BIST

To avoid the change of path delay or propagated values caused by excessive heating and power noise, the DART technology can provide a low power BIST method for test power reduction or control. Test power can be classified into three elements, test pattern input (scan-in), test (capture) and test pattern output (scan-out) powers, each of which have different behavior. The proposed low power BIST method is a holistic approach to solve all types of test power issues. Our low power BIST can be implemented by adding power reduction circuits for each test power as shown in Fig. 3-8. Figure 3-9 shows results comparing with some existing approaches. These results show that our low power BIST is effective not only for test power reduction but also for test quality improvement [16, 17].

3.6 DART Technology Case Study

A case study of the DART technology on industrial circuit is given in this section [15]. Target circuit has 7.2M gates, 356k flip-flops and 12 clock domains. It also has 264 memory blocks, including SRAMs and register files. Its DFT circuits for manufacturing test includes not only scan circuits but also TPG(Test Pattern Generator) and TRA(Test Response Analyzer) for logic BISR, circuits for BIST, and TAPC(Test Access Port Controller) for boundary scan.

Fig. 3-10 shows the design structure of the circuit with DART functionality. It embedded a test controller for DART, a test timing generator for delay measurement, an onchip DART memory for storing DART test information and test logs, and temperature and voltage monitors (TVMs) [13] for compensation of temperature and voltage impact on path delays. The DFT circuits, that is logic BIST circuits and memory BIST circuits, for manufacturing test are controlled through TAPC.

The results of this case study are as follows.
Table 3-1 Gate Overhead of DART Circuits

<table>
<thead>
<tr>
<th>Item</th>
<th># Cells</th>
<th>Comb. Circ.</th>
<th>Others</th>
<th>Total</th>
</tr>
</thead>
<tbody>
<tr>
<td>For LBIST</td>
<td>1.1k</td>
<td>2.0k</td>
<td>0.2k</td>
<td>2.2k</td>
</tr>
<tr>
<td>For MBIST</td>
<td>1.1k</td>
<td>1.6k</td>
<td>0.2k</td>
<td>1.8k</td>
</tr>
<tr>
<td>Overall Control</td>
<td>0.5k</td>
<td>0.2k</td>
<td>2.6k</td>
<td>2.8k</td>
</tr>
<tr>
<td>TVM</td>
<td>2.5k</td>
<td>6.8k</td>
<td>0.4k</td>
<td>7.2k</td>
</tr>
<tr>
<td>Total Overall</td>
<td>5.2k</td>
<td>10.5k</td>
<td>4.4k</td>
<td>13.9k</td>
</tr>
</tbody>
</table>

Table 3-2 Accuracy of Temperature and Voltage Estimation by TVMs

<table>
<thead>
<tr>
<th>Temperature Interval</th>
<th>-40°C ~ 20°C</th>
<th>20°C ~ 80°C</th>
<th>80°C ~ 110°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0V ~ 1.1V</td>
<td>Error (Min, Max)</td>
<td>-2.6°C ~ 2.4°C</td>
<td>-2.6°C ~ 2.4°C</td>
</tr>
<tr>
<td></td>
<td>Std. Div.</td>
<td>1.2°C</td>
<td>1.1°C</td>
</tr>
<tr>
<td>1.1V ~ 1.2V</td>
<td>Error (Min, Max)</td>
<td>-3.3°C ~ 3.0°C</td>
<td>-2.7°C ~ 2.6°C</td>
</tr>
<tr>
<td></td>
<td>Std. Div.</td>
<td>1.4°C</td>
<td>1.3°C</td>
</tr>
<tr>
<td>1.2V ~ 1.3V</td>
<td>Error (Min, Max)</td>
<td>-2.8°C ~ 1.9°C</td>
<td>-1.8°C ~ 1.9°C</td>
</tr>
<tr>
<td></td>
<td>Std. Div.</td>
<td>1.2°C</td>
<td>0.9°C</td>
</tr>
</tbody>
</table>

As shown in Table 3-1, the gate overhead for DART circuits is about 14k gates in total, which is less than 0.2% of whole circuit. It is noted that the on-chip DART memory is not included in the gate overhead since it can be used in common with work memory for ordinary function.

Table 3-2 shows the results on the accuracy of temperature and voltage estimation by TVMs. A two-stage estimation, that is interval estimation followed by precise estimation, is used to obtain the results of 0.7 to 1.4 °C standard deviation in temperature and 3 to 5 mV standard deviation in voltage.

In the experiments on the adjustability to test constraints (test data volume and test time) in field, not only all the 12 intra-domain circuits but also 52 inter-domain circuits are targeted for logic BIST. Two test constraints are considered, that is, 8kB for test data volume and 200ms for test time. The logic BIST for DART utilizes reseeding technique by multiple seed patterns for TPG to improve test quality. It is noted that the use of many seeds can improve test quality but it will increase test data volume. Table 3-3 shows the test data volume to test all target circuits at one test chance (NTC=1). Several cases of the number of seeds for each intra-domain circuit and for each inter-domain circuit are evaluated, but even for the minimum case, that is, 1 seed for each intra-domain and 1 seed for each inter-domain, the test data volume exceeds the test constraint. On the other hand, for the cases where the whole test set are divided into 8 subsets and apply one subset at each test chance by rotating test [8] (NTC=8), more seed can be used within the test constraint as shown in Table 3-4. In general, intra-domains are larger than inter-domains, and so if the number of seeds for each intra-domain is maximized, 22 seeds can be used for each intra-domain. Test time for each case are evaluated similarly, and the results for NTC=1 and NTC=8 are shown in Tables 3-5 and 3-6, respectively. Detailed conditions are not shown here but the results illustrate the effectiveness of rotating test for keeping test constraints.

Table 3-3 Estimated Test Data Volume (NTC=1)

<table>
<thead>
<tr>
<th># Seeds Intra-Domain</th>
<th>Test Data Volume</th>
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<tbody>
<tr>
<td>1</td>
<td>10kB</td>
</tr>
<tr>
<td>2</td>
<td>11kB</td>
</tr>
<tr>
<td>3</td>
<td>12kB</td>
</tr>
<tr>
<td>1</td>
<td>10kB</td>
</tr>
<tr>
<td>2</td>
<td>11kB</td>
</tr>
<tr>
<td>3</td>
<td>12kB</td>
</tr>
</tbody>
</table>

Table 3-4 Estimated Test Data Volume (NTC=8)

<table>
<thead>
<tr>
<th># Seeds Intra-Domain</th>
<th>Test Data Volume</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>4.8kB</td>
</tr>
<tr>
<td>2</td>
<td>5.6kB</td>
</tr>
<tr>
<td>5</td>
<td>8.0kB</td>
</tr>
<tr>
<td>22</td>
<td>7.9kB</td>
</tr>
</tbody>
</table>

Table 3-5 Estimated Test Time (NTC=1)

<table>
<thead>
<tr>
<th># Seeds Intra-Domain</th>
<th>Test Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>229ms</td>
</tr>
<tr>
<td>2</td>
<td>271ms</td>
</tr>
<tr>
<td>3</td>
<td>313ms</td>
</tr>
<tr>
<td>1</td>
<td>229ms</td>
</tr>
<tr>
<td>2</td>
<td>271ms</td>
</tr>
<tr>
<td>5</td>
<td>143ms</td>
</tr>
<tr>
<td>22</td>
<td>174ms</td>
</tr>
</tbody>
</table>

(c) Copyright 2012, 2013 All right reserved DART White Paper (Version 4.1)
Other experiments are executed for showing the effect of test quality improvement by reseeding. Three clock domains (T0, T2 and T7) are used for intra-domain test and a seed selection method [7] is applied. Figure 3-11 show the fault coverage curves for each clock domain by random BIST (1 seed) and BIST reseeding (multiple seeds) with seed selection. It can be seen that BIST reseeding can achieve higher fault coverage than random BIST in less test patterns for all cases. Though these experiments do not consider the test constraints above, the results imply that appropriate selection of seeds and appropriate division of whole test set considering circuit structure may lead to enough test quality within given test constraints.

![Fig. 3-11 Fault Coverage Improvement by Seed Selection](image)

3.7 DART Implementation Guideline

To ease the implementation of the DART technology on LSI, we develop **DART Implementation Guideline** (DART Guideline, in short) based on the results of the above researches and developments. The DART Guideline defines DART modules, which are key components to realize DART. Each DART modules can be realized as a software module or a hardware module. Fig. 3-12 illustrates the relation between DART modules and related modules shown in the DART Guideline.

![Fig. 3-12 DART Modules and Related Modules](image)

**DART Controller** (DART_CNT), which is provided as a software DART module, controls overall DART operation in field. DART_CNT accesses an external non-volatile memory (called DART External Memory), which stores all information of DART test and a record of test log data, and an embedded work memory (called DART Internal Memory (DART_MEM)), which stores specific test execution information and the test result log data. Moreover, DART_CNT determines specific test contents and calculates estimated/corrected value of temperature, voltage and circuit delay. Furthermore, DART_CNT triggers DART Test Controller (DART_TC) to start a DART test execution.
DART_TC, which is provided as a hardware DART module, controls all other hardware DART modules to execute a DART test. On the trigger from DART_CNT, DART_TC executes a DART test defined by the specific test execution information stored in DART_MEM by booting up a BIST (LBIST (logic BIST) or MBIST (memory BIST)) Controller for manufacturing test corresponding to a specified circuit under test (CUT). In case of LBIST, DART_TC updates test timing generated by DART Clock Generator (DART_CG) to measure the maximum operating frequency of the CUT. Both for LBIST and MBIST, DART_TC also boots up TV Monitor Controller (TVM_CNTL) to execute measurement by TV Monitor (TVM) to estimate temperature and voltage during the test. At the end of test, DART_TC write the test result log date in DART_MEM to pass the information to DART_CNT.

Some of the DART functionalities have already validated by the implementation on FPGA.

4. Other Activities

4.1 Activities for Standardization

There is a well-known international standard for functional safety, IEC61508, related to field reliability. It defines 'safety integrity level (SIL)' as a metric to express safety of electrical, electronic, or programmable electronic systems. There are four levels of SILs (SIL1-SIL4) and SIL4 is the highest level. IEC61508 Part2, Annex E gives a standard on on-chip redundancy, where the level of SIL3 is defined as follows.

\[ \beta_{IC} \text{ estimated susceptibility of IC with on-chip redundancy to common cause failures (CCFs)} \]

- initial value of \( \beta_{IC} = 33\% \)
  - increase based on Table E.1 and decrease based on Table E.2
  - if final \( \beta_{IC} < 25\% \), then SIL3

An example of increasing factor is a monitoring by on-chip watchdog (5\%), and an example of decreasing factor is a structure with isolating and decoupling physical locations (2-4\%). The DART technology can provide functionalities of detection of delay increase and prediction of degradation, and so it has good potential to strengthen the countermeasures of CCFs and hence decrease \( \beta_{IC} \). We will work for addition of these techniques to Table E.2 and also we will target the inclusion of them in the requirement of SIL4.

4.2 Intellectual Property

We can actively license our patents shown in Fig. 4-1 to promote the practical application of the DART technology.

![Field Test Architecture/Circuit](1) Appl.# 2010-057310
(2) WIPO WO2011/115038, Taiwan 100108218
(3) degradation detection

![Test Method - Circuit](1) Appl.# 2010-225318
(2) WIPO WO2012/046602
(3) high quality field test - BIST

![Test Method - Algorithm](1) Appl.# 2010-07003
(2) WIPO WO2011/086884, Taiwan 100101509
(3) high quality field test - temperature control

![Peripheral Patents](1) Appl.# 2010-138609
(2) WIPO WO2011/158500, Taiwan 100121280
(3) asynchronous circuit test for NoC/GALS

![Thermal/Voltage/Degradation Monitor](1) Appl.# 2012-002214
(2) WIPO WO2013/105564
(3) power-aware BIST

![Thermal/Voltage/Degradation Monitor](1) Appl.# 2011-008850
(3) aging-free monitor circuit

![Thermal/Voltage/Degradation Monitor](1) Appl.# 2011-065061
(3) degradation level calculation circuit

Fig. 4-1 DART Patent Map
5. Conclusion

As shown in this white paper, we have been developing an LSI test technology for supporting high field reliability. We have been proceeding some feasibility studies of the developed technologies, but we know the best way to validate the effectiveness of DART is collaborations to industries who really apply it in practice. We appreciate your cooperation.

DART Paper List

DART Technology White Paper (Version 4.1)

Issued on September 9, 2013

Issued by CREST-DVLSI Kajihara Team (Principal Co-Researchers)

<table>
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<tr>
<th>Research Director</th>
<th>Kyushu Institute of Technology</th>
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</thead>
<tbody>
<tr>
<td>Seiji Kajihara</td>
<td></td>
</tr>
<tr>
<td>Michiko Inoue</td>
<td>Nara Institute of Science and Technology</td>
</tr>
<tr>
<td>Yukiya Miura</td>
<td>Tokyo Metropolitan University</td>
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<td>Satoshi Ohtake</td>
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