The 21st Asian Test Symposium
Niigata, Japan
November 20, 2012

“VLSI design and testing for enhanced systems dependability”

浅井彰二郎
CREST/DVLSI 研究総括
（株）リガク取締役副社長

Shojiro Asai
Research Supervisor, CREST/DVLSI
Exec. VP and Director, Rigaku Corporation

Program term: FY2007~2014

The "Dependable VLSI Systems" is a collaborative university-industry research program funded by Japan Science and Technology Agency under the CREST* framework.

- In its 6th year of the 8 year term

•CREST: http://www.jst.go.jp/kisoken/crest/en/index.html

Rationale for research in DVLSI

VLSI: Key component of systems. Its dependability underlies systems dependability.

Problems: Threats to dependability is actually increasing.

Threats arising from miniaturization

Variations in dimensions, shape, doping,

Reduction in signal/noise (radiation, EMI, fixed and floating charge)

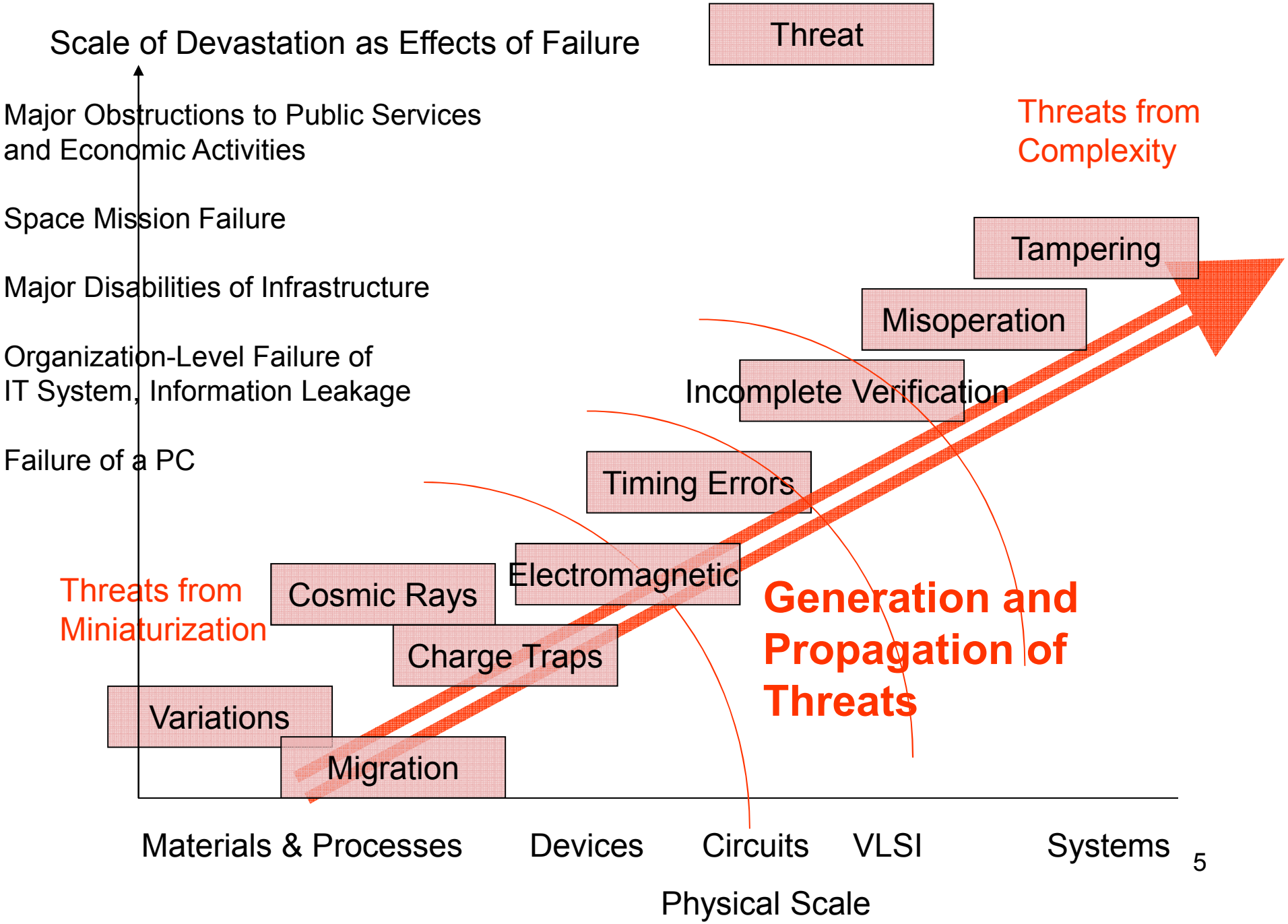
Aggravating wear/fatigue phenomena

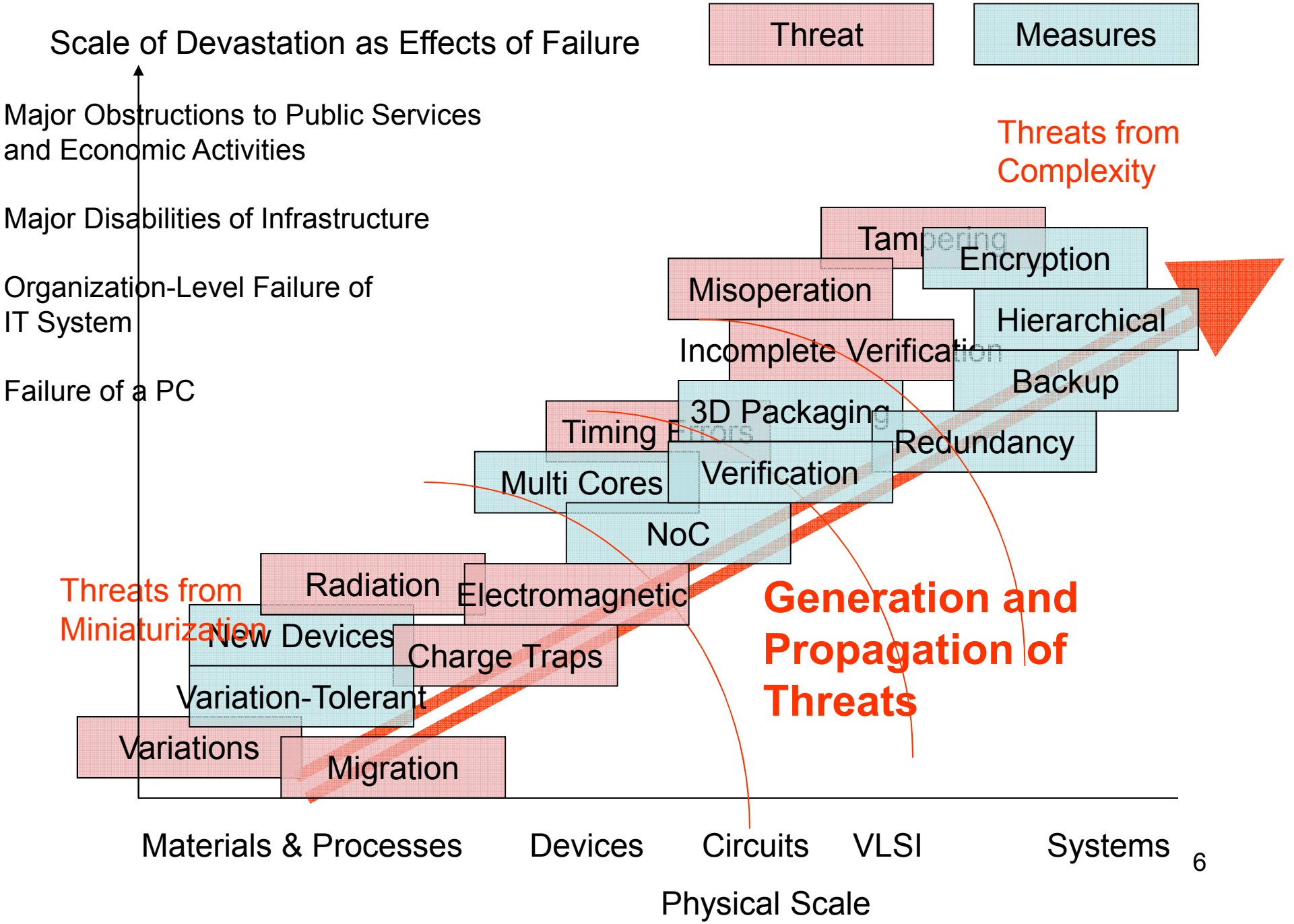
Threats from increased complexity

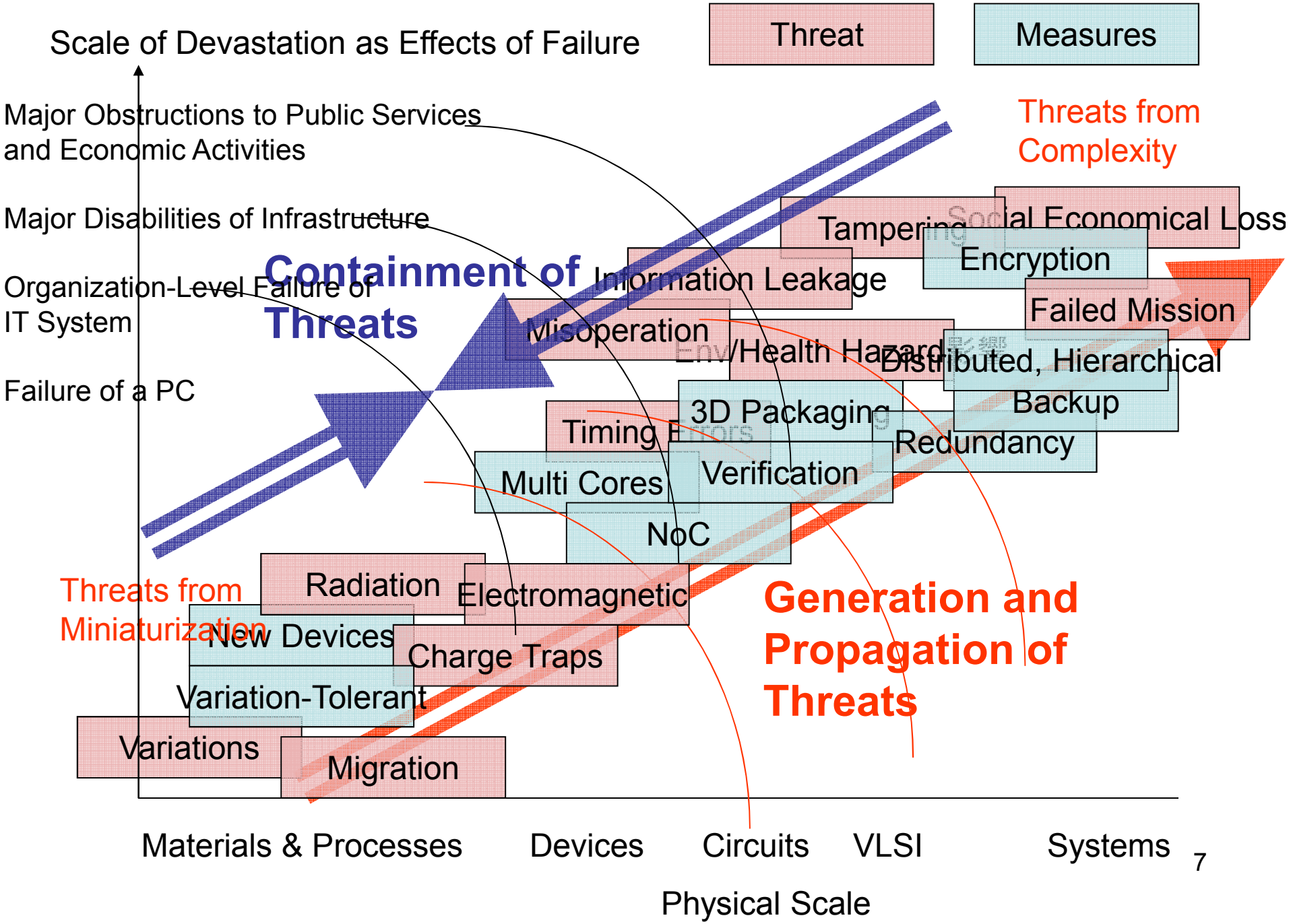
Enhanced functionality (id, encryption,---)

Multiple- Many-core architecture

Heterogeneous integration
Analog, digital, nonvolatile, network, sensors, actuators, etc.


Scale of Devastation as Effects of Failure
Threat
Major Obstructions to Public Services and Economic Activities
Space Mission Failure
Major Disabilities of Infrastructure
Organization-Level Failure of IT System, Information Leakage
Failure of a PC
Threats from Complexity
Tampering
Misoperation
Incomplete Verification
Timing Errors
Electromagnetic
Cosmic Rays
Charge Traps
Variations
Migration
Threats from Miniaturization
Generation and Propagation of Threats
Materials & Processes
Devices
Circuits
VLSI
Systems
Physical Scale


Scale of Devastation as Effects of Failure
Threat
Measures
Major Obstructions to Public Services and Economic Activities
Major Disabilities of Infrastructure
Organization-Level Failure of IT System
Failure of a PC
Threats from Complexity
Tampering
Encryption
Misoperation
Hierarchical
Incomplete Verification
Backup
3D Packaging
Timing Errors
Redundancy
Multi Cores
Verification
NoC
Threats from Miniaturization
Radiation
Electromagnetic
New Devices
Charge Traps
Variation-Tolerant
Variations
Migration
Generation and Propagation of Threats
Materials & Processes
Devices
Circuits
VLSI
Systems
Physical Scale


Scale of Devastation as Effects of Failure
Threat
Measures
Major Obstructions to Public Services and Economic Activities
Major Disabilities of Infrastructure
Organization-Level Failure of IT System
Failure of a PC
Threats from Complexity
Containment of Threats
Tampering
Social Economical Loss
Encryption
Information Leakage
Failed Mission
Misoperation
Env/Health Hazard
Distributed, Hierarchical
3D Packaging
Backup
Timing Errors
Redundancy
Multi Cores
Verification
NoC
Threats from Miniaturization
Radiation
Electromagnetic
New Devices
Charge Traps
Variation-Tolerant
Variations
Migration
Generation and Propagation of Threats
Materials & Processes
Devices
Circuits
VLSI
Systems
Physical Scale

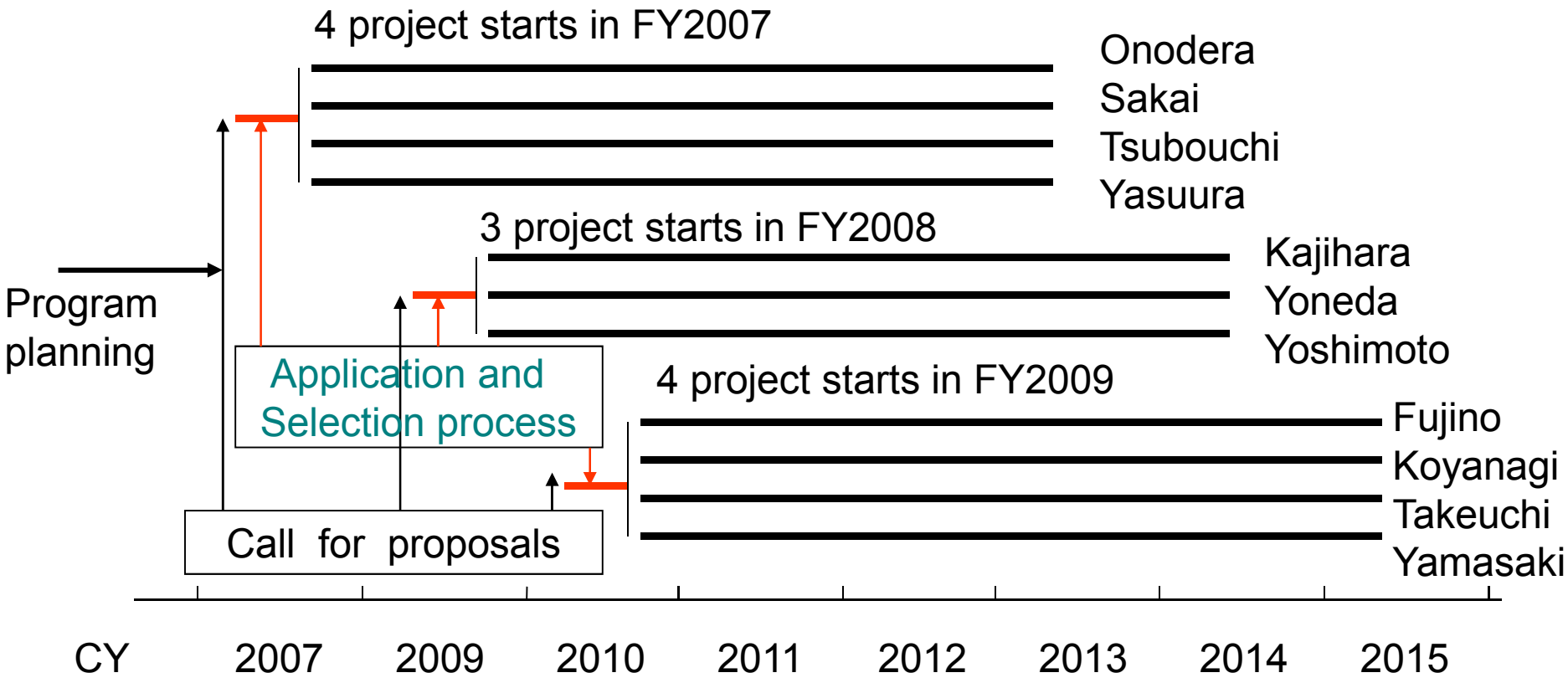
Mission of the DVLSI Program:

1. Contain Rising Threats within VLSI (Component Supposed to be Most Dependable)

2. Provide New Functionalities in VLSI which Improve Dependability at the Systems Level

Japan Science and Technology Agency

Selection and Terms of the DVLSI Projects



Program Term: 2007- 2015

Team #1 Hidetoshi Onodera , Kyoto University, PI,

Co-Investigators

Takao Onoye (Osaka Univ.)
Yukio Mitsuyama (Kochi Inst. Technol.)
Kazutoshi Kobayahi (Kyoto Inst. Technol.)
Hajime Shimada (NAIST)
Hiroyuki Kanbara (ASTEM)
Kazutoshi Wakabayashi (NEC)

Dependable VLSI Platform Using Robust Fabrics

Robust Fabric
Variability-Tolerant Flip-Flop
Radiation-Hard Flip-Flop
Fine-Grain Voltage-Frequency Control

Reconfigurable Processor Architecture
Coarse-Grain, Redundant Multiple Processors
Fine-Grain State Machine and
Application Development Environment in HDL (ANSI-C)

Team #2 Shuichi Sakai, The University of Tokyo), PI

Co-Investigators

Masahiro Fujita, The Univ. Tokyo
Kenji Kise The Univ. Tokyo
Kazutoshi Wakabayashi, NEC

Ultra Dependable VLSI by Collaboration of Formal Verifications and Architectural Technologies

Equivalence Verification
Post-Si Debugging and Patchable Design
Fault-Tolerant FPGA Architecture with a Small Redundant Configuration Circuit
Timing-Error-Tolerant Super-Scalar Processor
Dynamic Time-Borrowing Clocks in FPGA to Mitigate Timing Errors
Scalable Many-Core Tiles with Multiple-Function Routers
Interfacing CyberWorkBench, a Synthesis Tool, with FLEC, Equivalence Verification Tool

Team #1 Kazuo Tsubouchi, Tohoku University, PI

Co-Investigators

Akira Matsuzawa, Tokyo Institute of Technology
Makoto Iwata, Kochi University of Technology
Minoru Fujishima, Hiroshima University
Hiroshi Oguma, Toyama National College of Technology
Masatoshi Nakayama, Mitsubishi Electric Corporation

Dependable Wireless System and Device

Heterogeneous Air-Interfaces for Dependable Connection
  Cellular, WLAN, Short-Range
Frequency Domain Equalizer
Scalable A/D and D/A Converters
All-Si High-Frequency Amplifiers

Team #4 Hiroto Yasuura, Kyushu University, PI

Co-Investigators

Yusuke Matsunaga, Kyushu Univ.
Makoto Sugihara, Toyohashi Univ. Sci. and Technol.
Toshinori Sato, Fukuoka Univ.

Modeling, Detection, Correction and Recovery Techniques for Unified Dependable Design

EDA Tool Chain to Evaluate and Help Enhance Dependability
Covering from Physics up to Systems, RTL Level
Radiation-Induced Soft Errors considered as Threat

Timing Error Mitigation using ‘Canary’ Flip-Flops

Team #5 Seiji Kajihara, Kyushu Institute of Technology, PI

Co-Investigators
Michiko Inoue, NAIST
Masatoshi Otake, Oita University
Yukiya Miura, Tokyo Metropolitan University

Circuit and System Mechanisms for High Field-Reliability

Testing of VLSI in the Field for Enhanced Dependability
- Monitoring Circuit Delay during Run-Time, Turning-On, Turning-Off
- NBTI, Hot-Carrier Injection, Electro-migration, etc
- Predicting Failure and Allowing Preventive Maintenance

Reliability Assessment during Development

Accuracy in Field Environment
On-Chip and Off-Chip IP
Data Logging

Help Reduce 'Undetected Dangerous' Failures (Common-Cause Failure)

White Paper

Team #6 Tomohiro Yoneda, National Institute of Informatics, PI

Co-Investigators

Masashi Imai, Hirosaki University
Atsushi Matsumoto, Tohoku University
Takahiro Hanyu, Tohoku University
Hiroshi Saito, Aizu University
Kenji Kise, Tokyo Institute of Technology

Dependable Network-on-Chip Platform

Seamless On-Ship and Inter-Chip Links for Multiple- or Many-Core Systems
- Demonstration in multiple ECU for automotive applications
- Dual modular redundancy

4 V850E Cores + 4 NoCs in 130nm integrated on a chip to demonstrate the concept.

Team #7 Masahiko Yoshimoto, Kobe University, PI

Co-Investigators

Makoto Nagata, Kobe University
Koji Nii, Renesas Electronics
Yasuo Sugura, Hitachi, Ltd.
Shigeru Oho, Nippon Institute of Technology

Dependable SRAM Techniques for Highly Reliable VLSI System

Dependable SRAM for Dependable System
- QoB (Quality-of-Bit, 14T Cell)
- Fine-Grain Voltage Control

Fine-Grain Voltage-Frequency Control
6T Cell Layout for Multiple-Cell-Upset Tolerance
Fault-Injection into SRAM and Systems-Level Simulation: Virtualization
Automotive Applications

Team #8 Takeshi Fujino (Ritsumeikan University), PI

Co-Investigators	Yohei Hori, AIST Masaya Yoshikawa, Meijo University Daisuke Suzuki, Mitsubishi Electric

The Design and Evaluation Methodology of Dependable VLSI for Tamper Resistance

AES Cryptographic Module Dual-Rail RSL Memory

The SASEBO (Side-channel Attack Standard Evaluation Board)
More than 100 units have been distributed to provide a standard testing environment for testing robustness against side-channel attack

Team #9 Mitsumasa Koyanagi, Tohoku University, PI

Co-Investigators

Hiroaki Kobayashi, Tohoku University
Takafumi Aoki, Tohoku University
Toshinori Sueyoshi, Kumamoto University
Tadashi Kamata, Denso

Three-Dimensional VLSI System with Self-Restoration Function

3D LSI
High Speed Parallel Processing for Image Recognition
On-Line Self-Test
System Level Supervisor controlling BIST
Quadruple-Redundant TSVs
Fault-Tolerant TMR

Team #10 Ken Takeuchi, Chuo University, PI

Co-Investigators Tadahiro Kuroda, Keio University
Hiroki Ishikuro, Keio University

Dependable Wireless Solid-State Drive (SSD)

Terabyte capacity NAND flash memory
Robust against cell error, contact error, EMI, ESD. Waterproof

High-speed near-field wireless communication 10Gbps (2012), 50Gbps (2014) at 1mm distance

Wireless power delivery with MHz load variability

Team #11 Nobuyuki Yamasaki, Keio University, PI

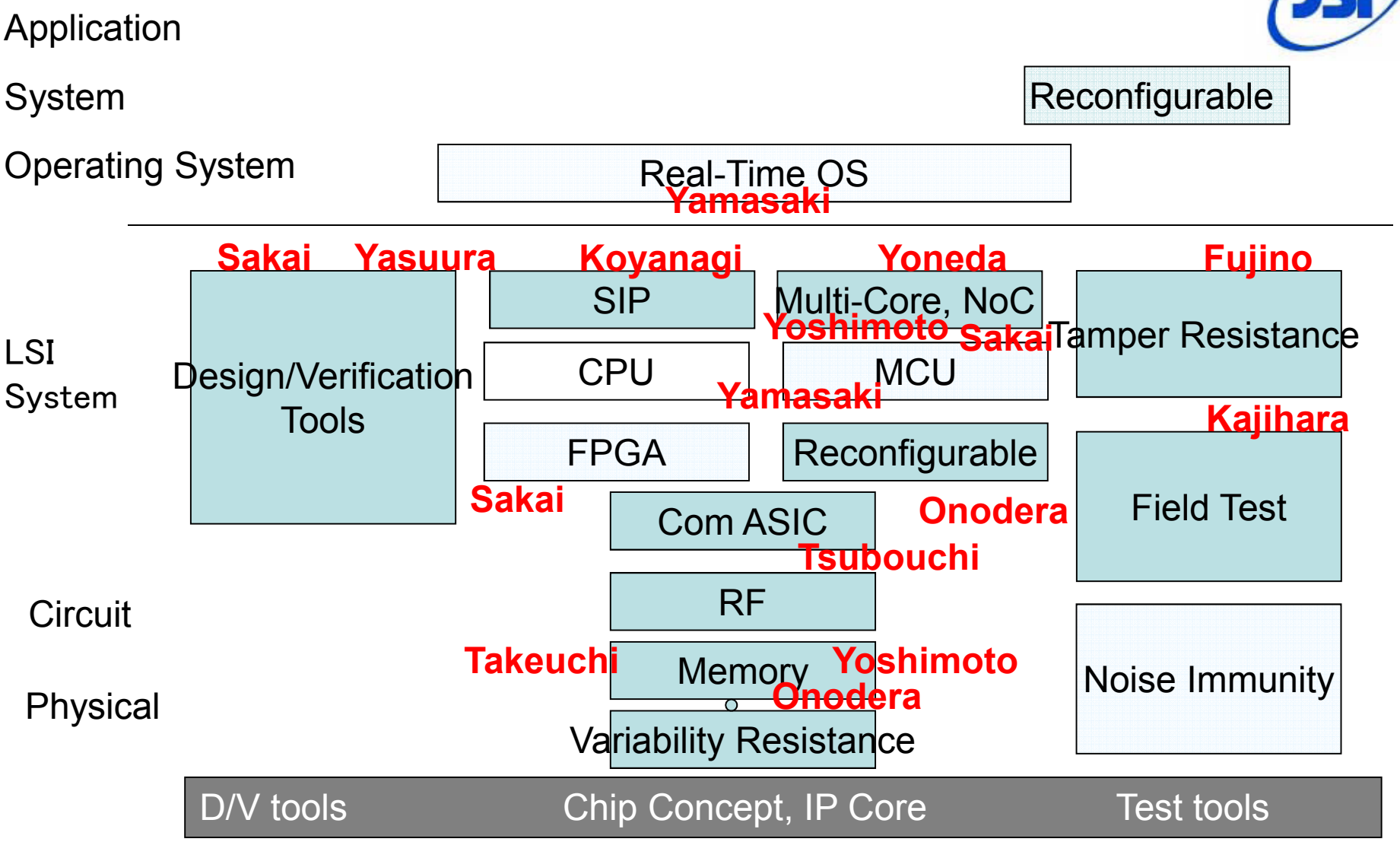
Co-Investigators Masayuki Inaba, The University of Tokyo
Kikuo Wada, NEC-AT

Fundamental Technology on Dependable SoC and SiP for Embedded Real-Time Systems

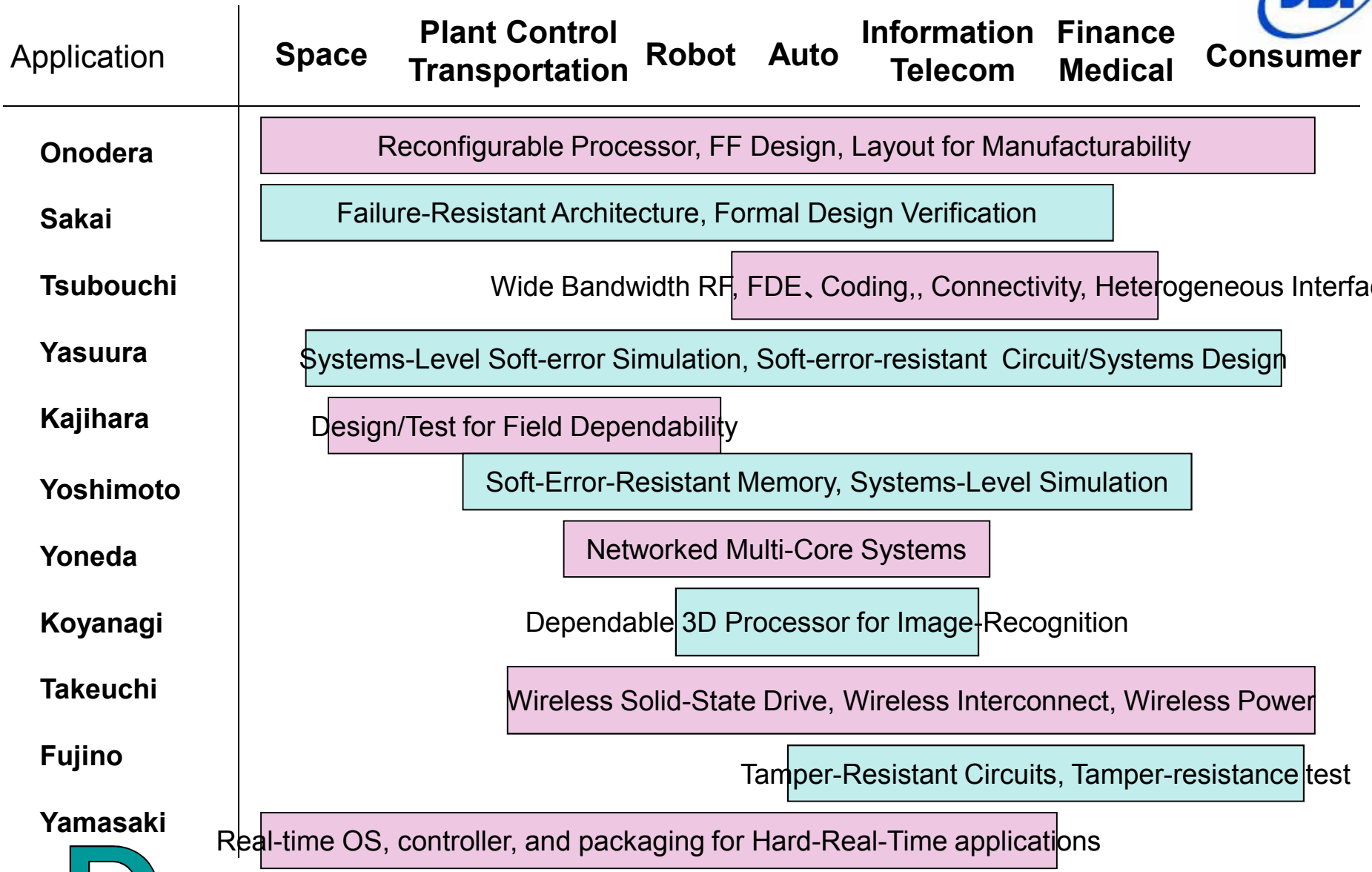
Robots

Hard-Real-Time Embedded Control System
Dynamic Real-Time Multiple-Thread Processor
control cycle time: 10 μs (cf ca 1ms currently available)
Responsive Link inter-device synchronization time of 100 μs (cf 8ms of USB)
operable under extremely high noise environment
low static power consumption 1W for the whole logic (cf ca 80W current)
small module size 20 mm sq
vertical chip stacking
Being verified in a humanoid robot.
Evaluation Kit

Areas DVLSI Projects cover:



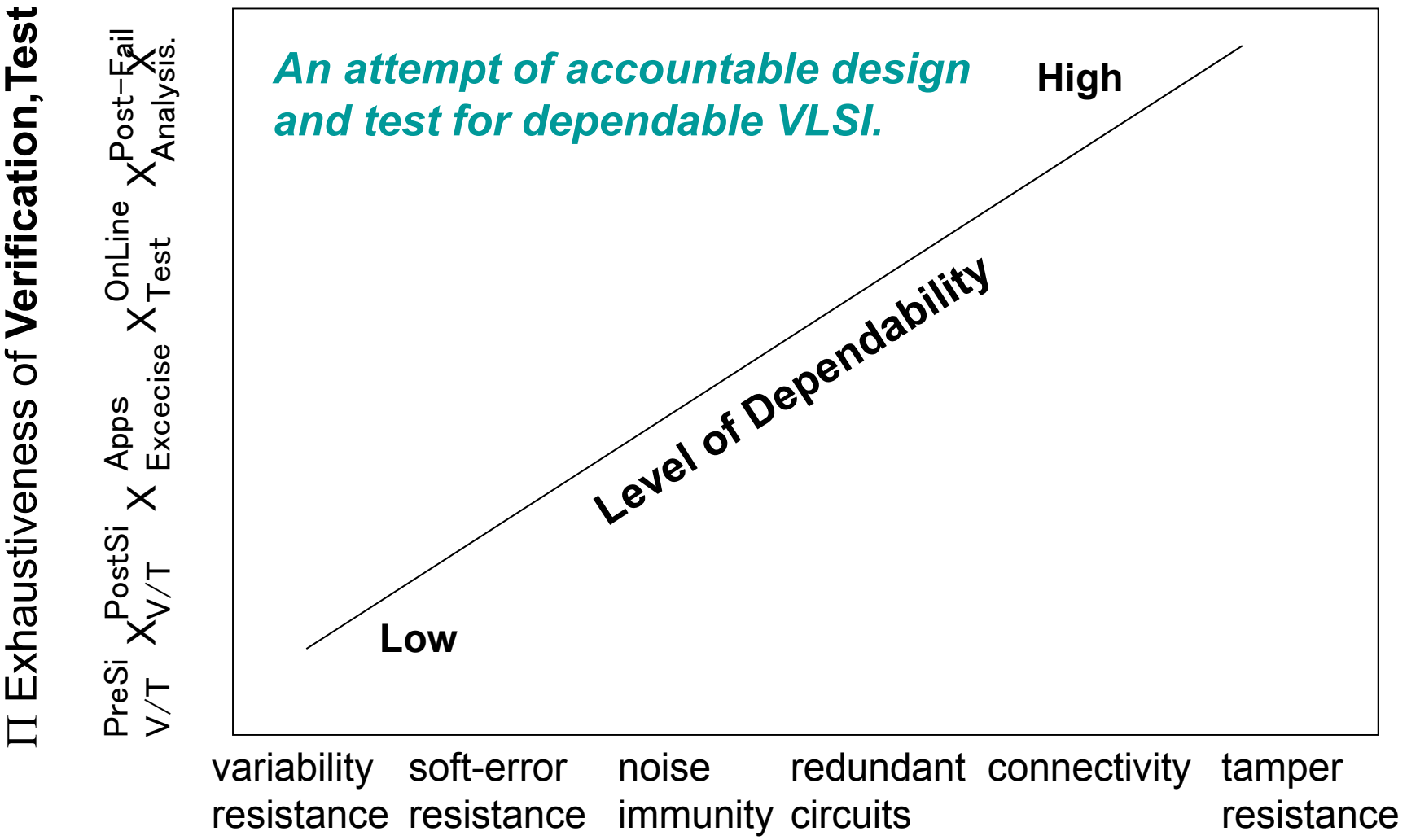
Applications eyed and Approaches taken



Attributes, Threats, and Means in Dependability as defined by IFIP:

Attributes	way to assess the dependability of a system
Availability	readiness for correct service
Reliability	continuity of correct service
Safety	absence of catastrophic consequences on the users/environment
Integrity	absence of improper system alteration
Maintainability	ability for a process to undergo modifications and repairs
Threats	things that can affect the dependability of a system
Fault	defect in a system
Error	discrepancy between the intended and actual behavior of a system
Failure	system behavior that is contrary to its specification
Means	ways to increase a system's dependability
Prevention	preventing faults being incorporated into a system
Removal	fault removal during development and removal during use
Forecasting	prediction of faults to remove them or circumvent their effects
Tolerance	putting fault-tolerant mechanisms in place

VLSI Dependability = Π (Strength of Means against Threat) x Π (Coverage of Verification and Test)



Π Strength of **Means** against Threat (Robustness of Technology)

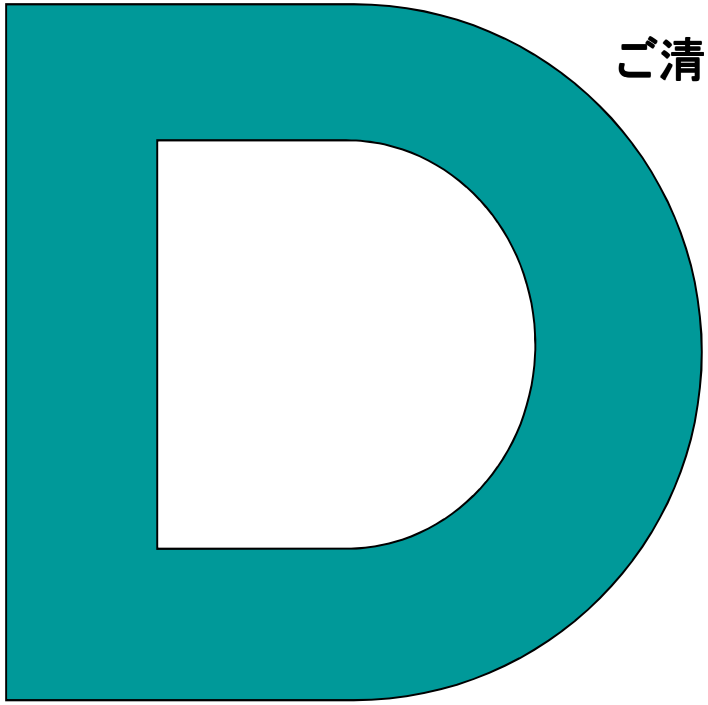
Japan Science and Technology Agency

The JST International Symposium on Dependable VLSI 2012

9:00 – 19:00 Saturday, December 2012
Akiba Hall, Tokyo

Invited Talks by Experts from Round the World
Project Reviews
Demos and Posters
Panel Session

Thank you!



ご清聴ありがとうございました

For more details, please visit the URL:
http://www.dvlsi.jst.go.jp/
http://www.dvlsi.jst.go.jp/english/index.html