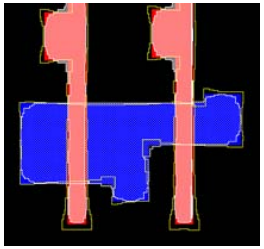
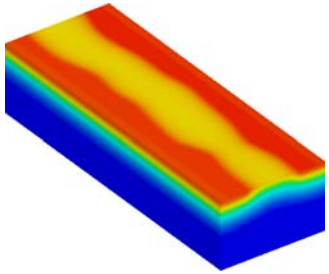
ロバストファブリックを用いたディペンダブルVLSIプラットフォーム

京都大学　小野寺秀俊

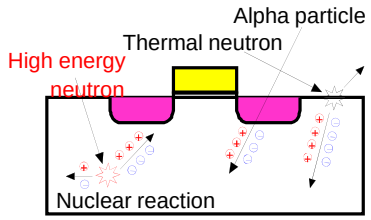
- 研究課題: 微細化に伴う物理的・自然現象的フォールトへの対応



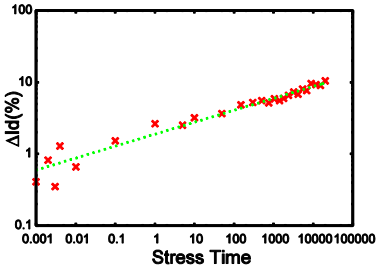
製造性劣化



特性ばらつき



ソフトエラー



経年劣化

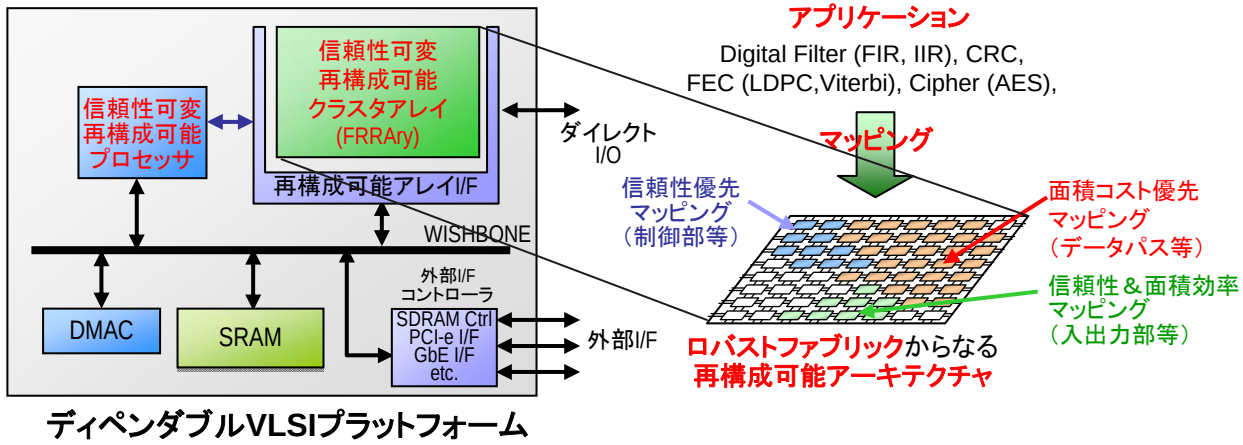
ITRS2009 Design Chapter

Table DESN1　Overall Design Technology Challenges

Challenges ≥ 22nm	*Summary of Issues*
Design productivity	System-level: high level of abstraction (HW/SW) functionality spec, platform based design, multi-processor programmability, system integration, AMS co-design and automation
	Verification: executable specification, ESL formal verification, intelligent test bench, coverage-based verification
	Logic/circuit/physical: analog circuit synthesis, multi-objective optimization
	Logic/circuit/physical: SiP and 3D (TSV-based) planning and implementation flows
	Heterogeneous component integration (optical, mechanical, chemical, bio, etc.)
Power consumption	Logic/circuit/physical: dynamic and static, system- and circuit-level power optimization
Manufacturability	Performance/power variability, device parameter variability, lithography limitations impact on design, mask cost, quality of (process) models
	ATE interface test (multi-Gb/s), mixed-signal test, delay BIST, test-volume-reducing DFT
Reliability	Logic/circuit/physical: MTTF-aware design, BISR, soft-error correction
Interference	Logic/circuit/physical: signal integrity analysis, EMI analysis, thermal analysis

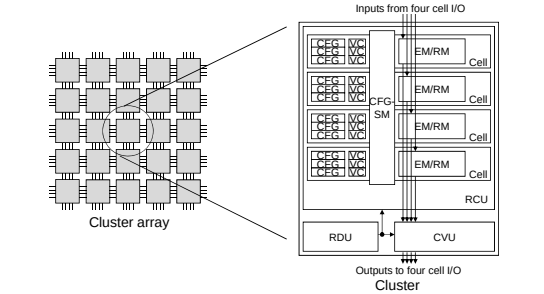
ロバストファブリックを用いたディペンダブルVLSIプラットフォーム：　研究成果と出口戦略

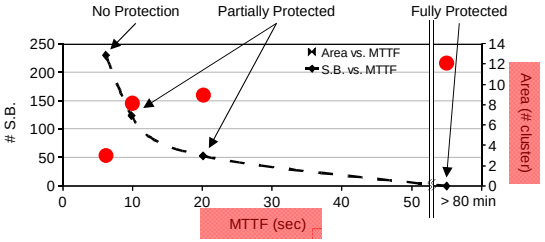
レイアウト/回路/アーキテクチャ/設自動化技術の階層横断的取り組み



ディペンダブルVLSIプラットフォーム

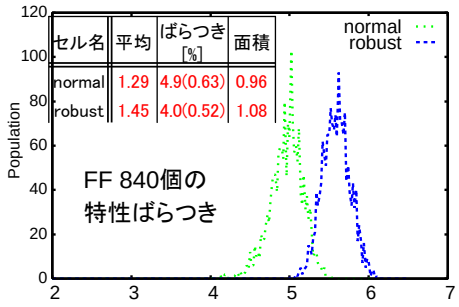
- 再構成可能アーキテクチャ(信頼性可変)



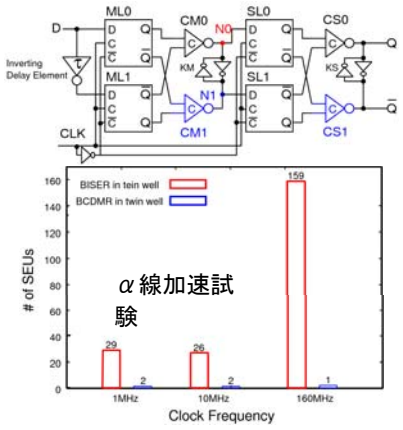


α線加速実験(65nmテストチップ)

- ロバストファブリック: Si-verified IP.　Available NOW
  - 耐ばらつきFF
  - 耐放射線FF

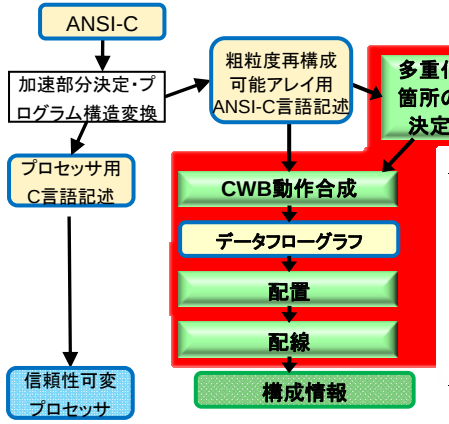


最大動作周波数[AU](40nm)



70万倍の放射線耐性(65nm)

- アプリケーション開発環境の提供(開発中)



CWBによる動作合成
- ANSI準拠C言語からの開発環境
- 面積、遅延制約を考慮した高位合成

マッピングツール
- 選択的多重化への対応

信頼性評価環境
- SEU耐性の定量的評価