Dependable VLSI Platform using Robust Fabrics

Director

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Principal Researchers

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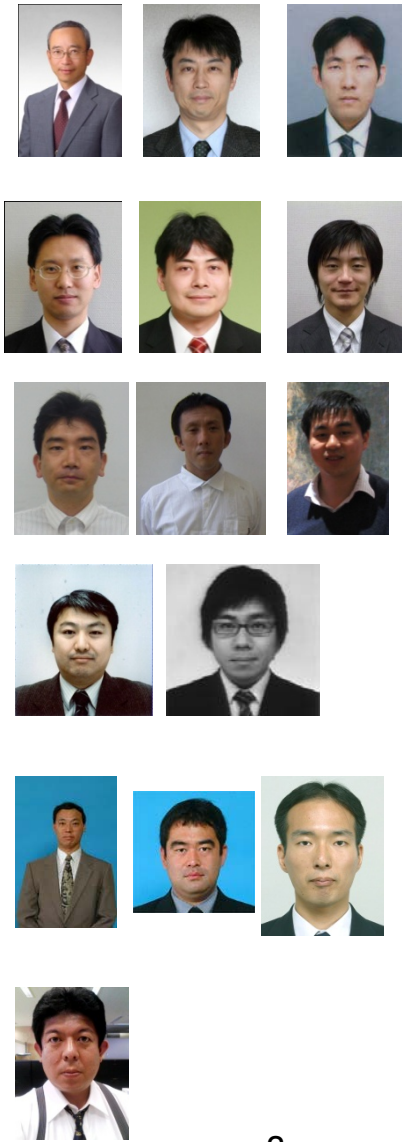
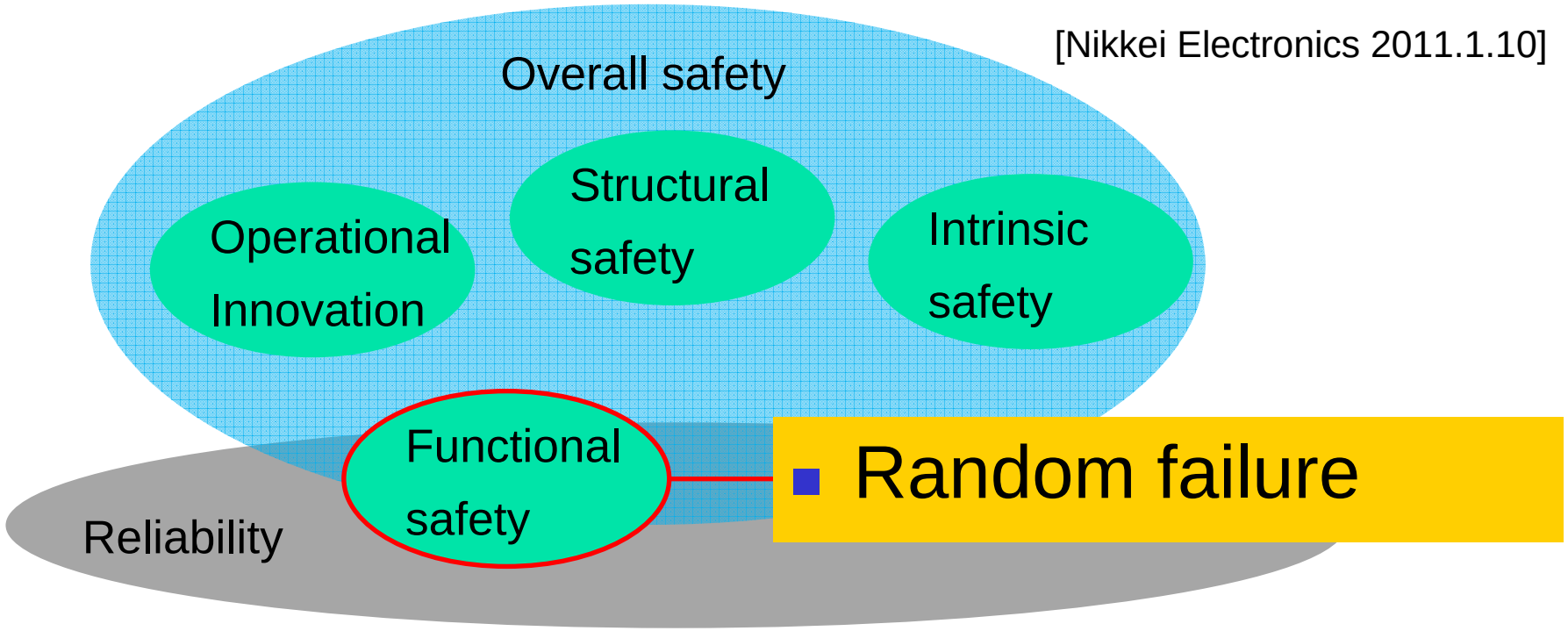
Whole Research Group

- Robust Fabric
  - Library-level Reliability
  - Onodera, Sato, Tsuchiya (Kyoto U.)
- Reconfigurable Architecture
  - FRRARY: Hardware-accelerator-level Reliability
  - Onoye, Hashimoto (Osaka U.), Mitsuyama (Kochi U. Tech)
- Reliable Processor
  - DARA: Processor-architecture-level Redundancy
  - BCDMR: Circuit-level Redundancy.
  - Kobayashi (Kyoto IT), Shimada, Yao (NAIST)
- Mapping Tools
  - Reliable Mapping
  - Ochi, Tsutsui (Kyoto U.)
- C-based Mapping Tools
  - Mapper for FRRARY
  - Wakabayashi, Takenaka, Noda (NEC)
- Applications
  - Dependability Evaluations and Applications for Reliability
  - Kanbara (ASTEM)



Our Approach to ISO26262

[Nikkei Electronics 2011.1.10]



- For random failures (‘soft-errors’) and self-recovering.
  - FRRARY(cluster array for hardware accelerator)
  - DARA (processor core)
- To reduce random failures
  - BCDMR-FF (Robust Flip-Flop)

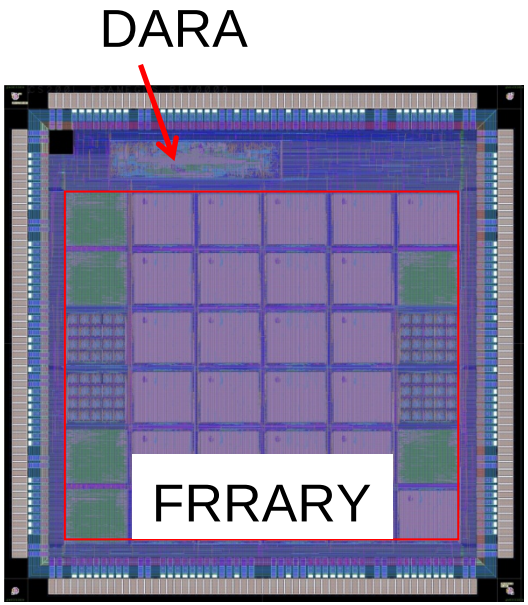
SoC for Dependable Platform

Functional Safety

- FRRARY (Flexible Reliability Reconfigurable Array)
  - Reconfigurable Hardware-accelerator-level Redundancy
- DARA (Dynamic Adaptive Redundancy Architecture)
  - Processor-architecture-level Redundancy
  - Pipeline-level Reliability Check

Reduce random failures

- BCDMR FF (Bistable Cross-coupled Dual Modular Redundancy FF)
  - Circuit-level Redundancy
  - Robust to alpha-particle and neutrons

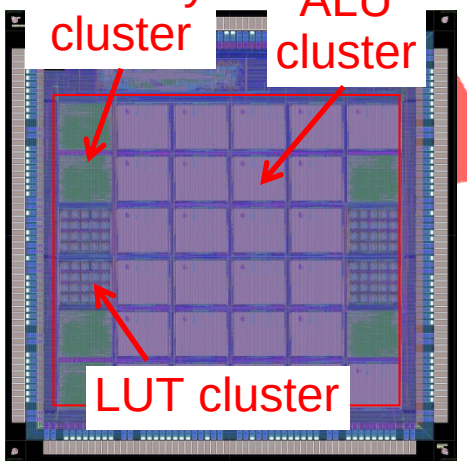


65nm 4mmx4mm Chip

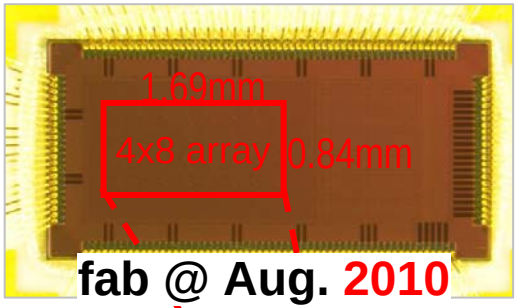
Mar. 2012 TO, will be fabricated Aug. 2012

Flexible Reliability Reconfigurable Array (FRRARY)

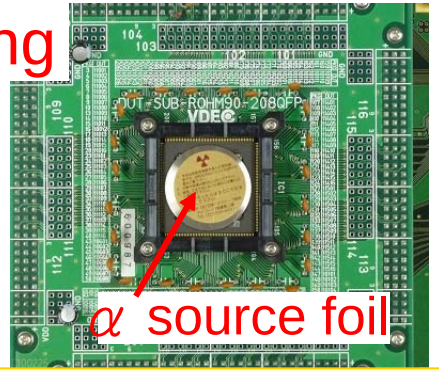
Coarse-grained reconfigurable architecture
offering flexible reliability to soft error and aging



fab. @ Aug. 2012

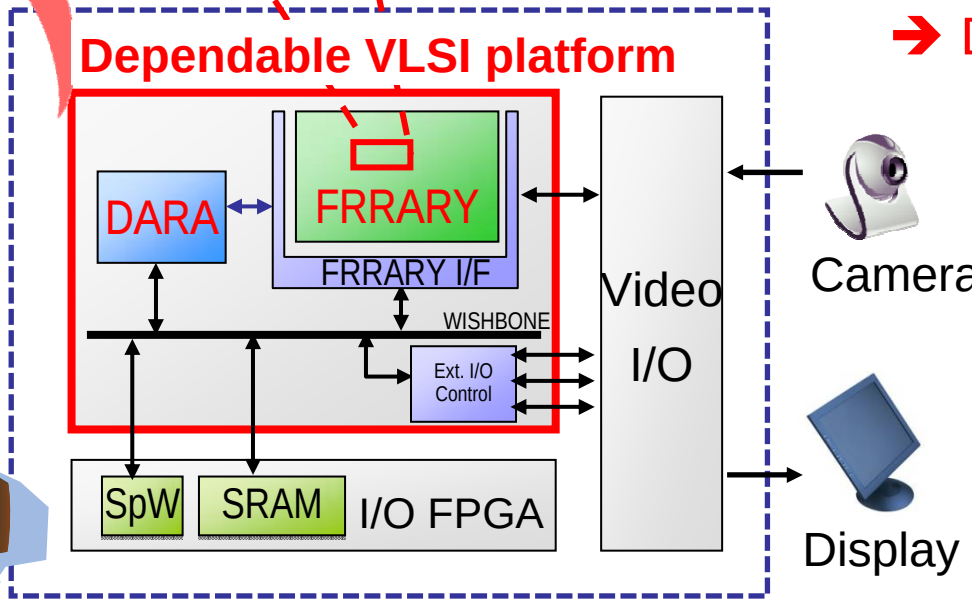


fab @ Aug. 2010

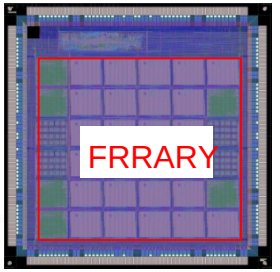


Accelerated radiation test

➔ Demo movie



Advantages of FRRARY

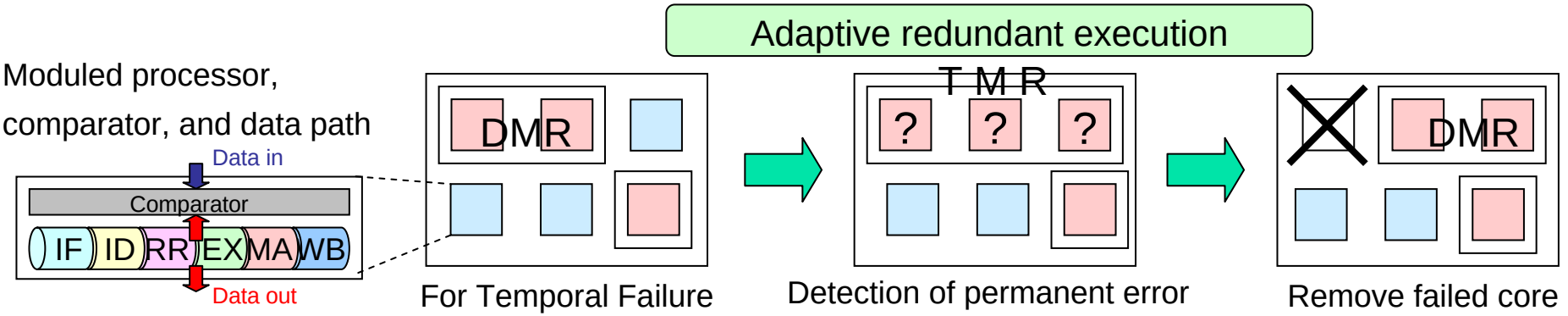


- Reconfigurable architecture-level Redundancy
  - Adaptively changes redundancy according to required reliability

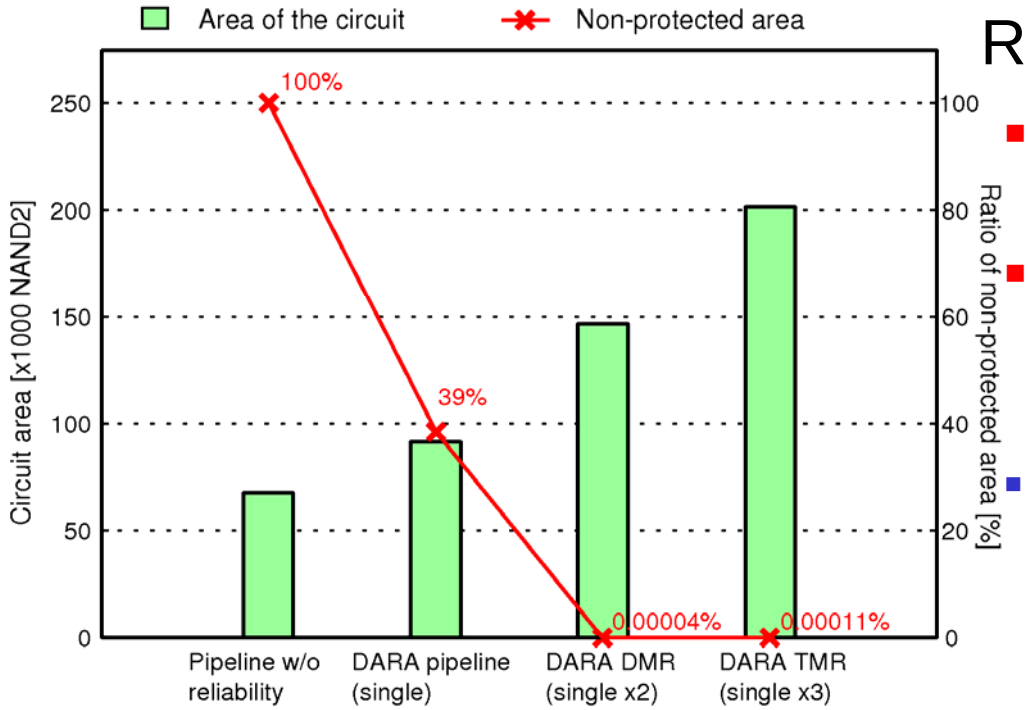
- Configuration data size is considerably smaller than that of FPGAs
  - Almost 1% of FPGAs ➔ 100x soft error resiliency

➡ FRRARY can achieve over 78000x reliability

Reliable Pipeline Processor : DARA

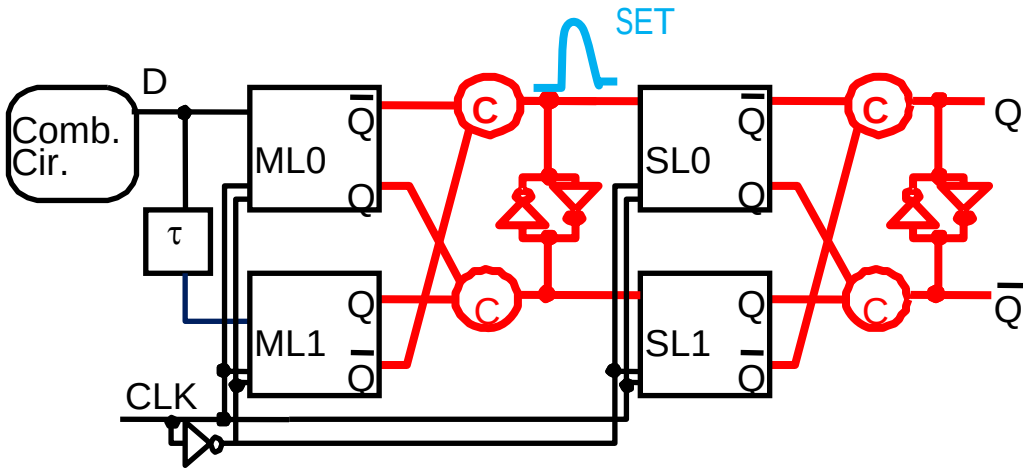


Area/Reliability Tradeoff



- DARA: Dynamic Adaptive Redundant Architecture
  - Duplicatable pipeline processor cores with comparators
  - Adaptive Redundancy
    - DMR for temporal failure
    - TMR for permanent failure
  - A test chip results using 180nm LSI
    - 360x MTTF than single pipeline

Robust FF: BCDMR FF



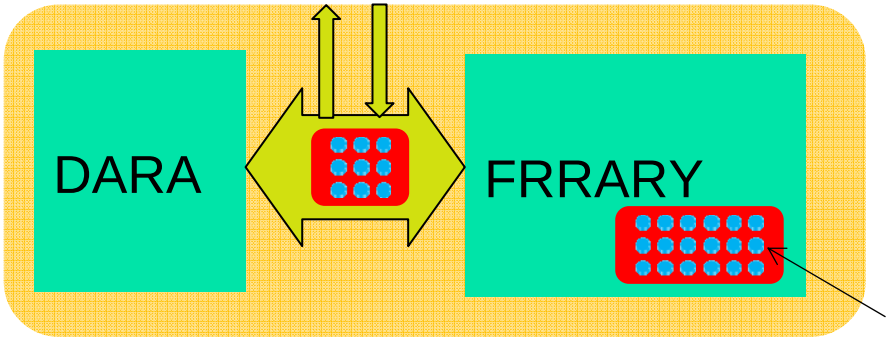
D-FF 1031FIT/Mbit

	well	Clock Freq.[MHz]			
		1	10	100	300
BISER	2	2	3	5	24
	3	1	1	6	12
BCDMR	2	0(<9) 260x			-
	3	3	2	2	-

Results from Neutron Irradiation (FIT/Mbit)

- Bistable Cross-coupled Dual Modular FF
  - Redundant FF for soft errrors based on BISER (Intel, Stanford)
  - No error is observed in BCDMR on twin (2) well
    - 260x stronger than D-FF

Flexible but Dependable Platform



Existing IPs

Cannot be changed at Arch/ RT level.

BCDMR

Dependability=min(FRRARY, DARA, BCDMR)

A weak component dominates Dependability

- DARA: Processor-level Dependability
- FRRARY: Reconfigurable Dependability
- BCDMR: Circuit-level Dependability
  - Whole circuit cannot be protected by architecture & processor-level

Summary

- Our Approach
  - FRRARY+DARA
    - Functional Safety
  - BCDMR FF
    - Reduce rate of random failures

Dependability=min (FRRARY, DARA, BCDMR)

=min(78k, 360, 240)

=at least 240x dependability

Architecture to Circuit-level (Overall) dependability

Brand-new Report from DAC2012

DAC community takes care of Dependability

- Panel Discussion
  - “Will Reliability be the Death of Moore's Law?”
    - Physical threats to dependability: Aging, Thermal Effects, Variability etc.
- Two Oral Sessions
  - “Facing Dependability: System-Level Solutions and Cybercar Challenges
    - Run-Time Adaptivity rather than at lower abstraction
  - “Yielding in an Uncertain World”
    - Solution below 22nm at manufacturing level