Dependable Memory Techniques for Highly Reliable VLSI System

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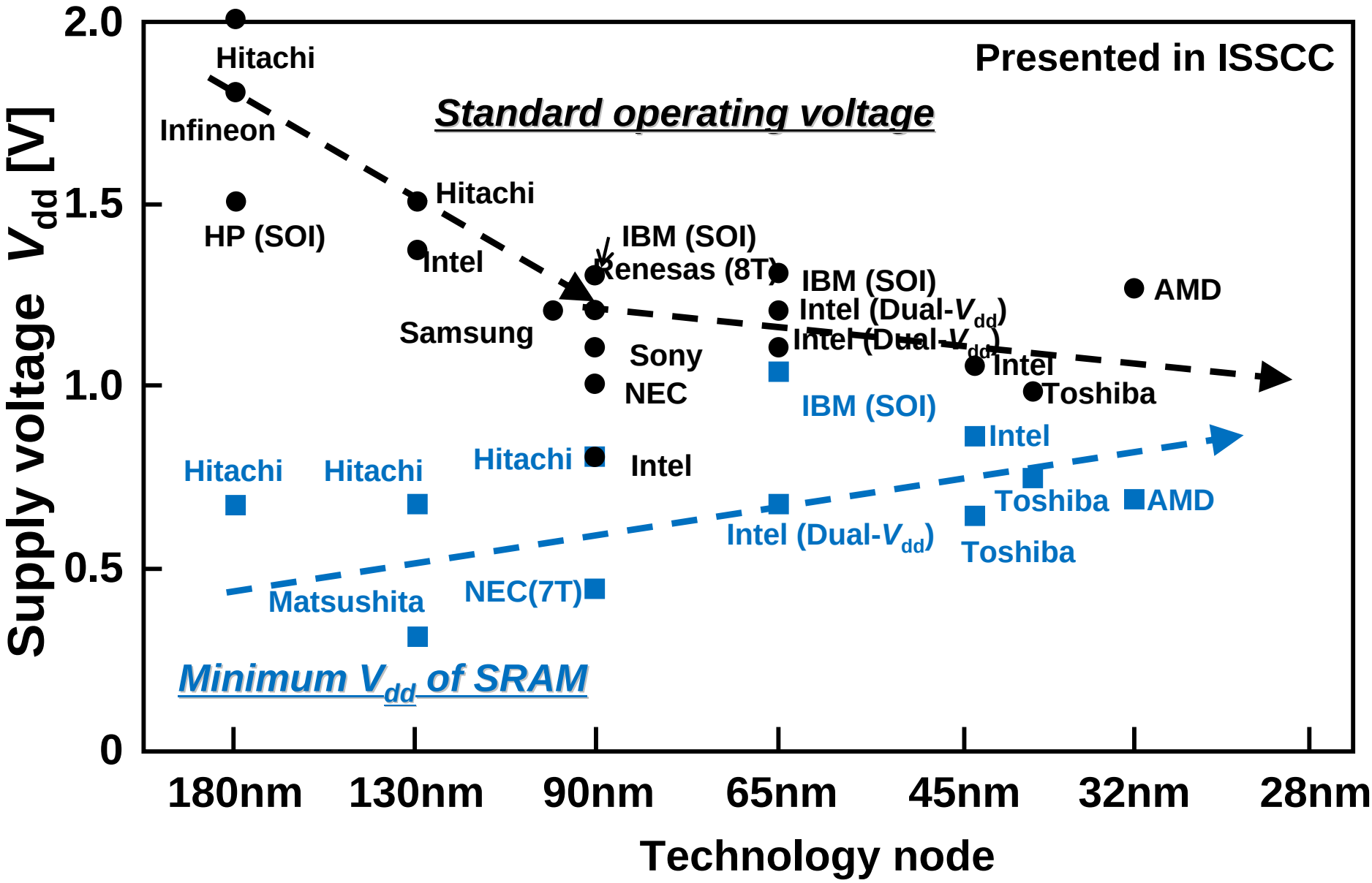
Dependability degradation factor

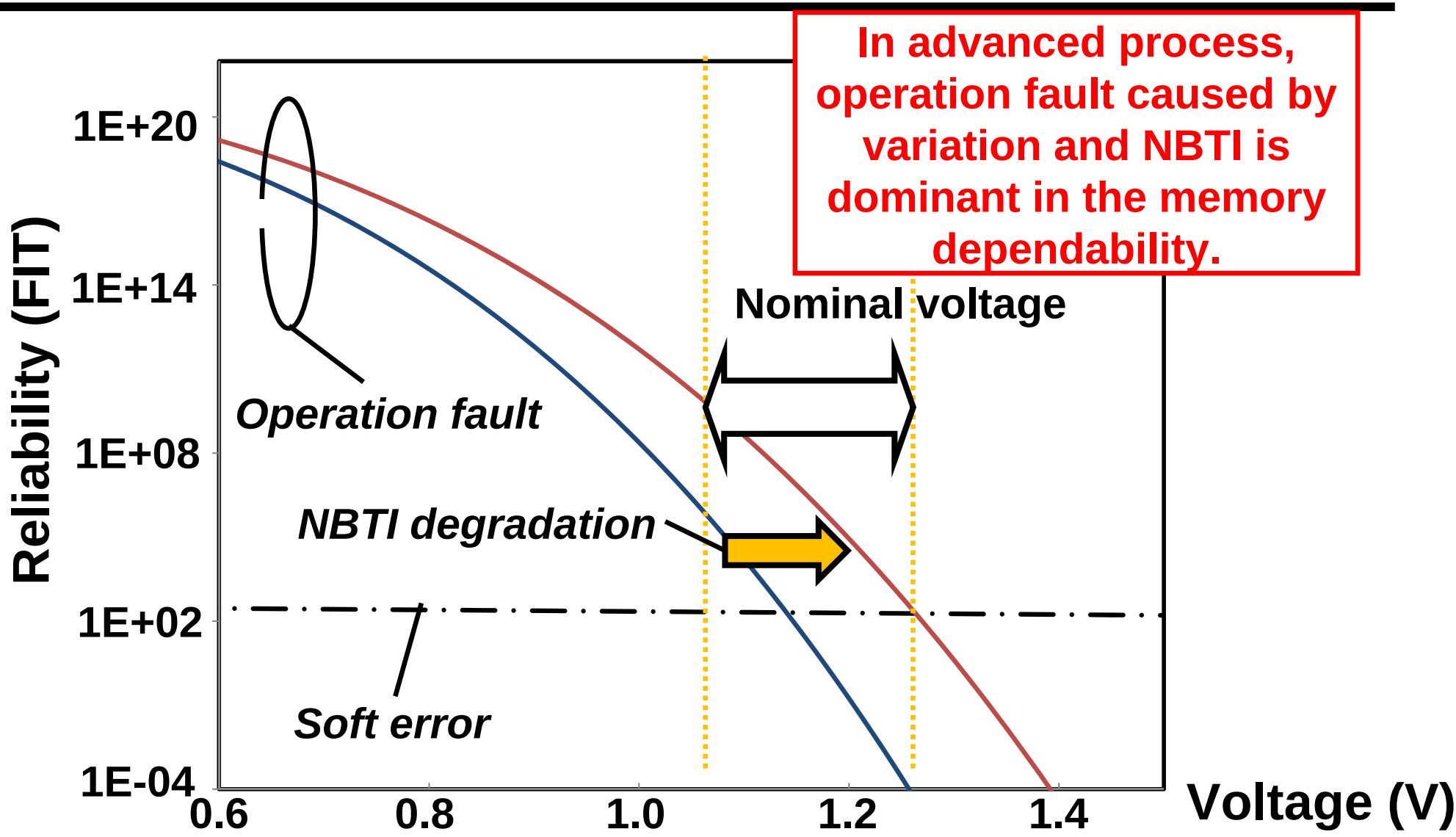
Dependability degradation factor	Improvement / tolerant technique
V_{th} variation	• QoB Cache • FGVC memory (with BIST)
NBTI, temperature fluctuation	
Power supply noise	• Power supply noise filter • Autonomic dependable memory with ODM
Soft error	• Soft error tolerant memory cell • Lockstep with QoB multicore

QoB: Quality of Bit
FGVC: Fine-Grain Voltage Control

SRAM operating voltage trend



Dependability evaluation with operation fault and soft error

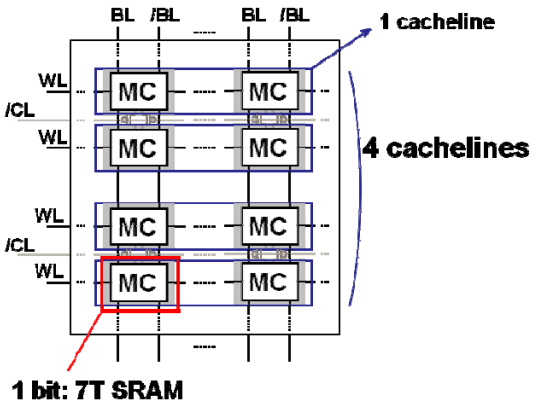


Margin improvement and soft error tolerant technique is necessary.

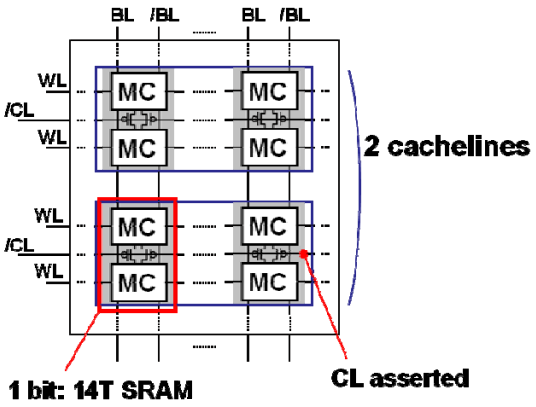
Associatively-Reconfigurable Cache with QoB SRAM

Proposed cache memory

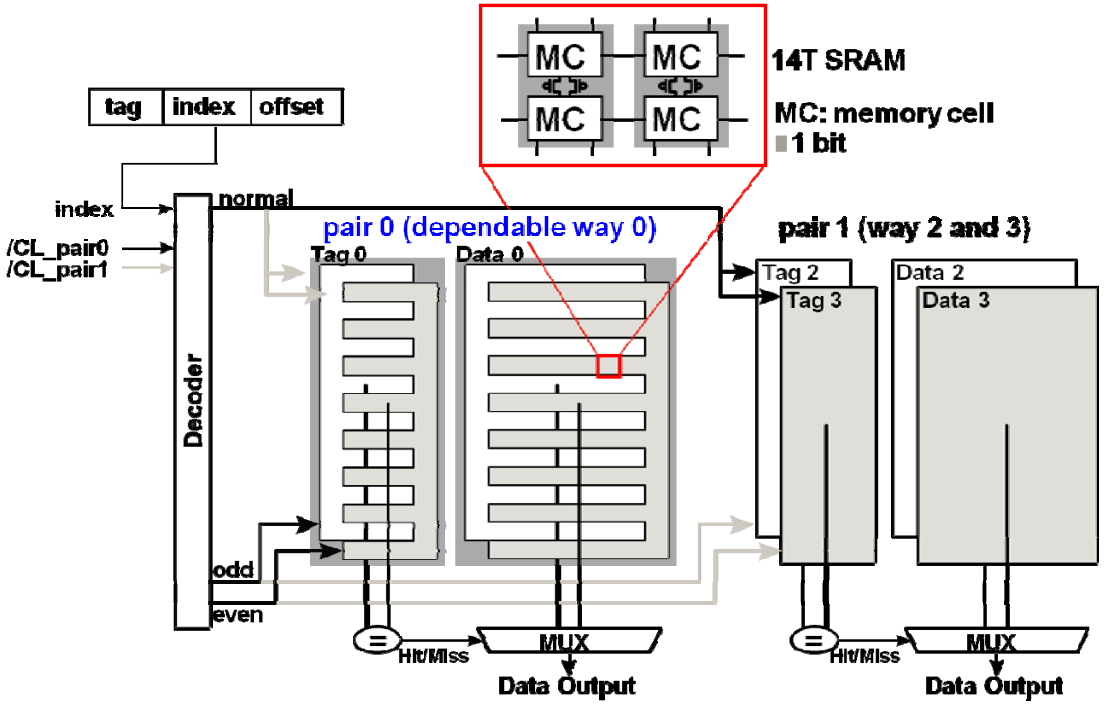
Normal mode operation



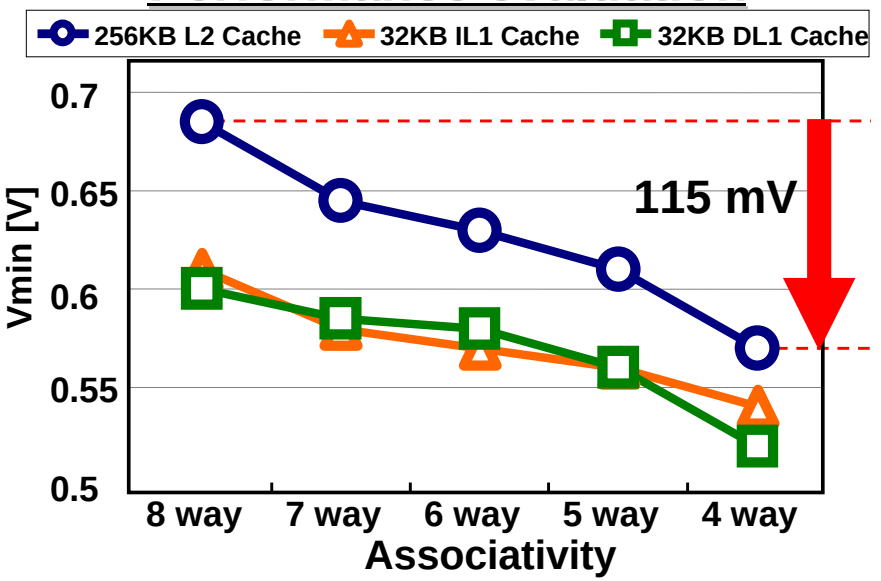
Dependable mode operation

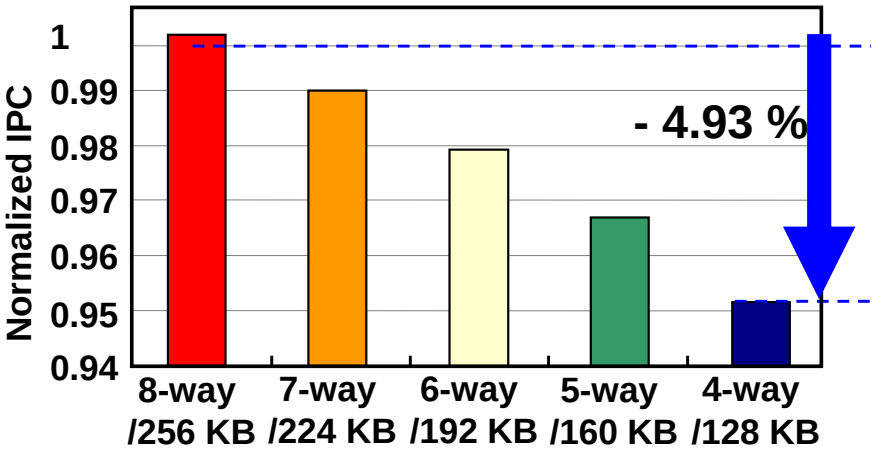


Consist one dependable way in dependable mode operation by pair structure of cache ways and QoB SRAMs



Minimum op. voltage and Performance evaluation

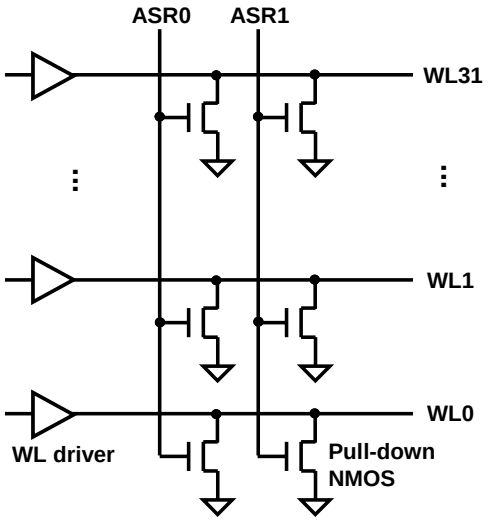




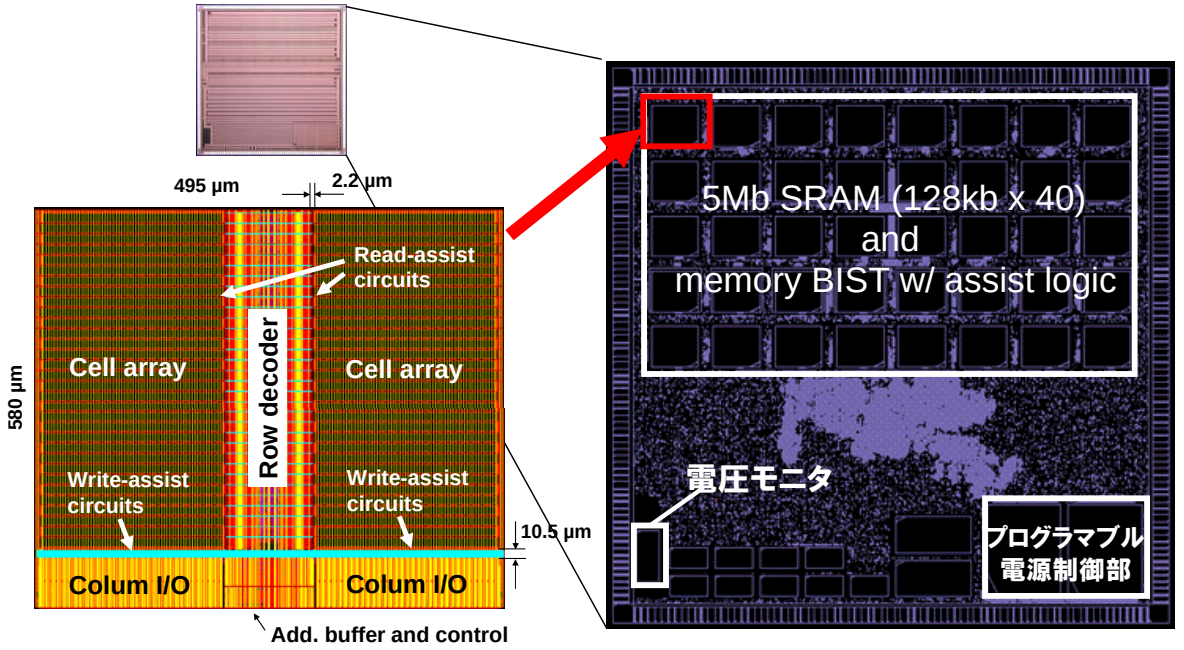
115 mV Vmin improvement with only 4.93% IPC degradation

Prop. cache can trade off processor performance for reliability

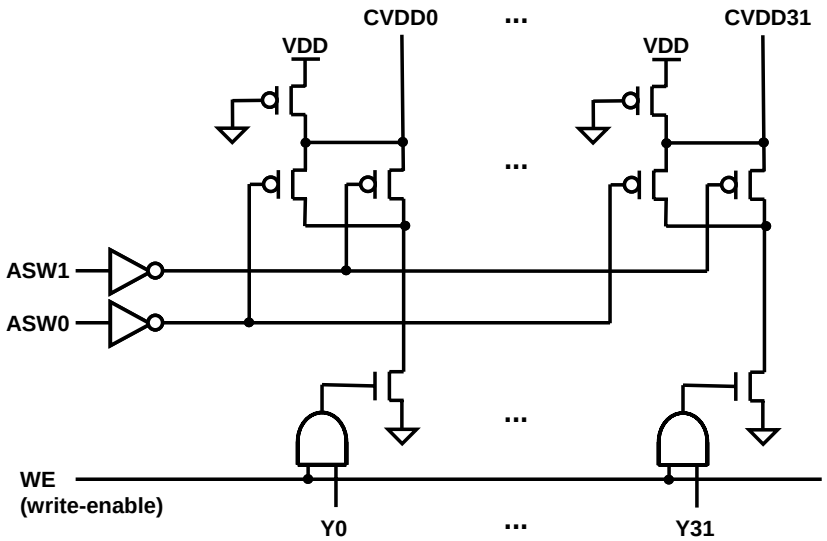
Fine Grain Voltage Control (FGVC) SRAM



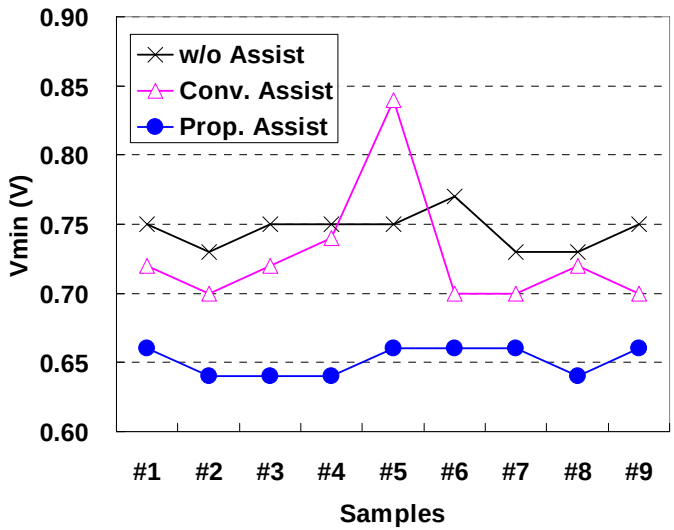
Read assist circuit



TEG chip and 128-Kb SRAM layout



Write assist circuit



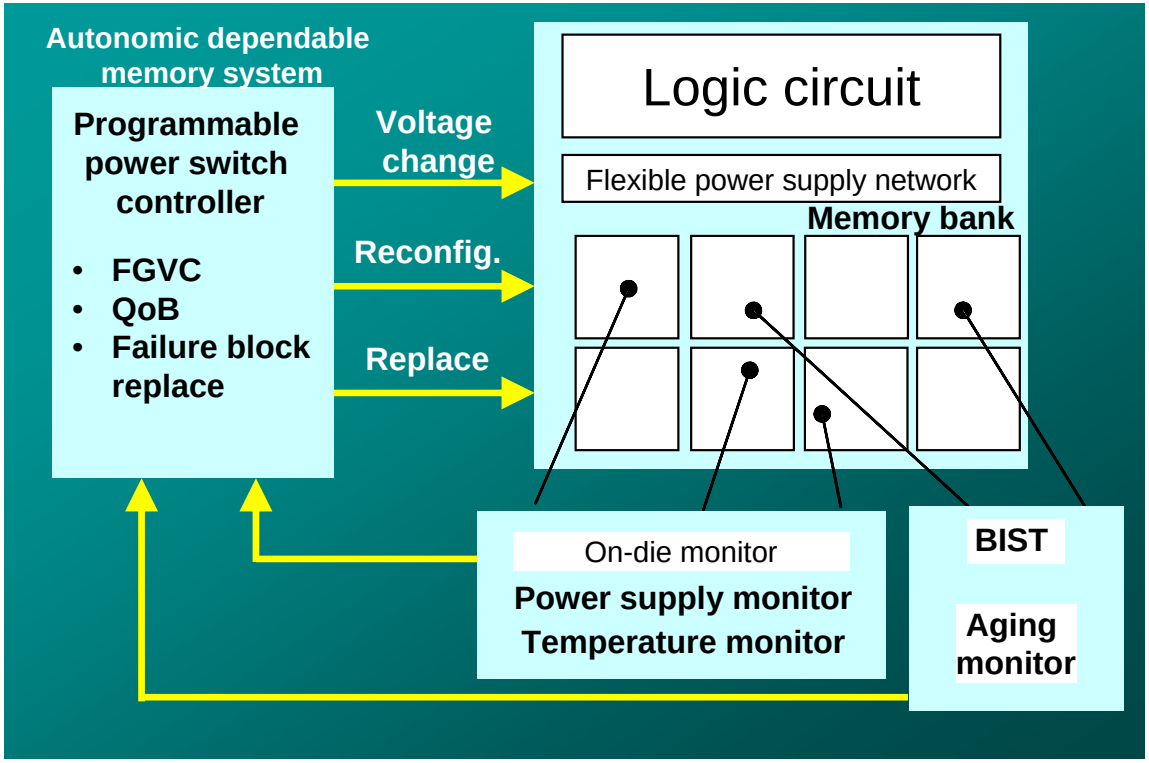
Measurement result

Autonomic dependable memory chip

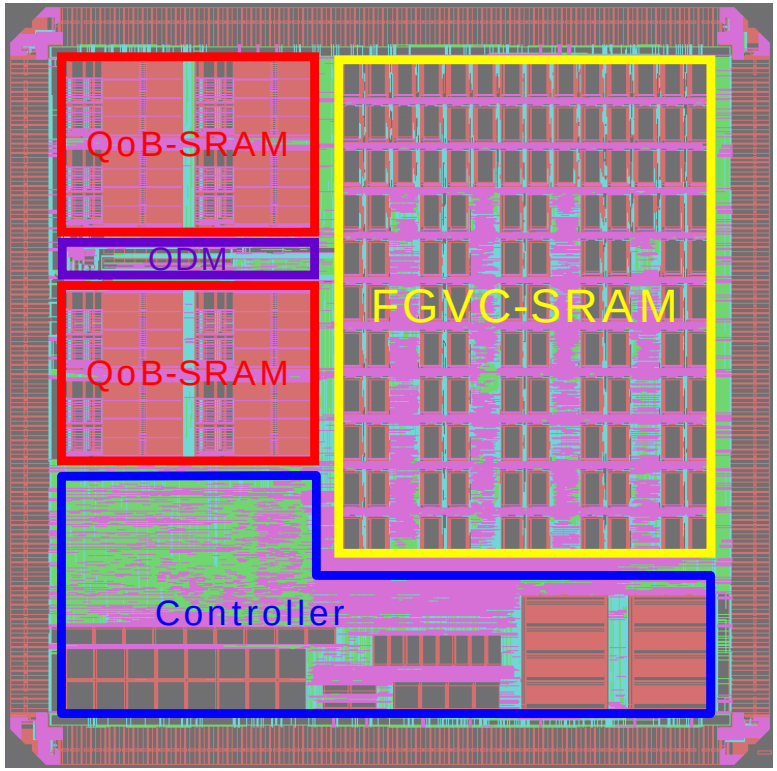
Confirmation of SRAM margin improvement scheme and failure detect technique.

- QoB-SRAM and FGVC-SRAM are implemented.
- Autonomic control logic applying BIST and power supply noise monitor are combined with QoB and FGVC SRAM.

Block diagram

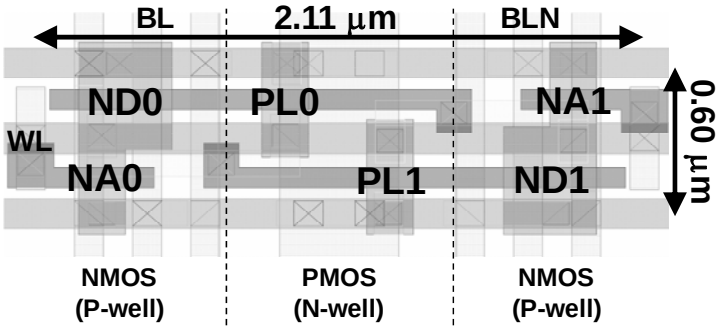


Chip layout

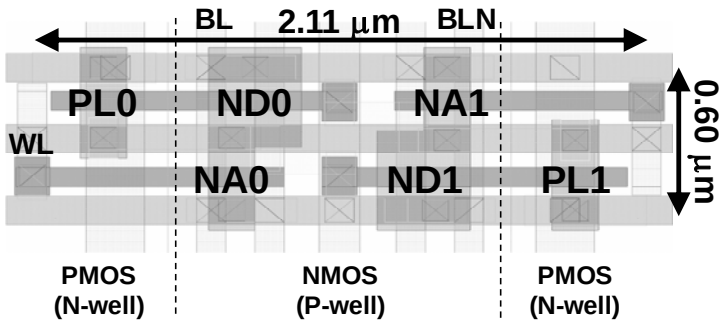


(40nm process, 5mm x 5mm)

MCU tolerant 6T SRAM cell layout



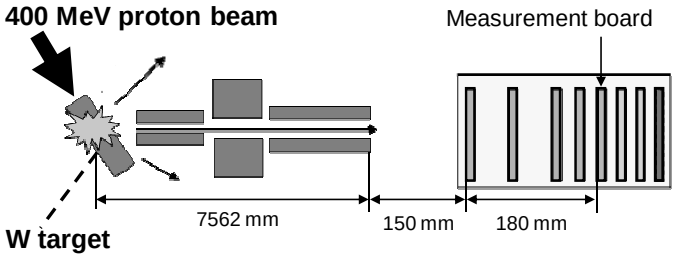
(a) Conventional NPN 6T cell



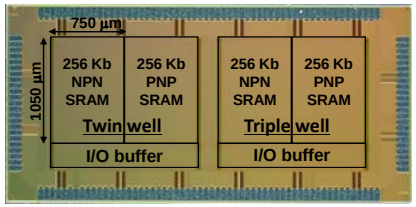
(b) Proposed PNP 6T cell

PMOS-NMOS-PMOS (NMOS-inside) 6T SRAM cell layout is proposed

The proposed layout mitigates horizontal multiple cell upset (MCU)



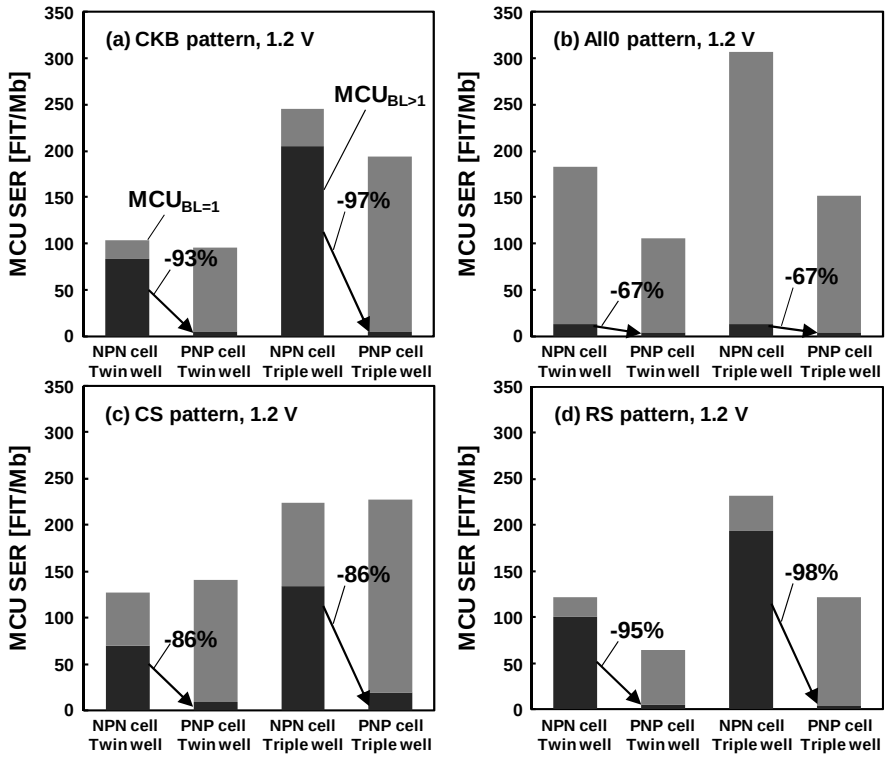
Neutron acceleration test at RCNP



1Mb SRAM TEG

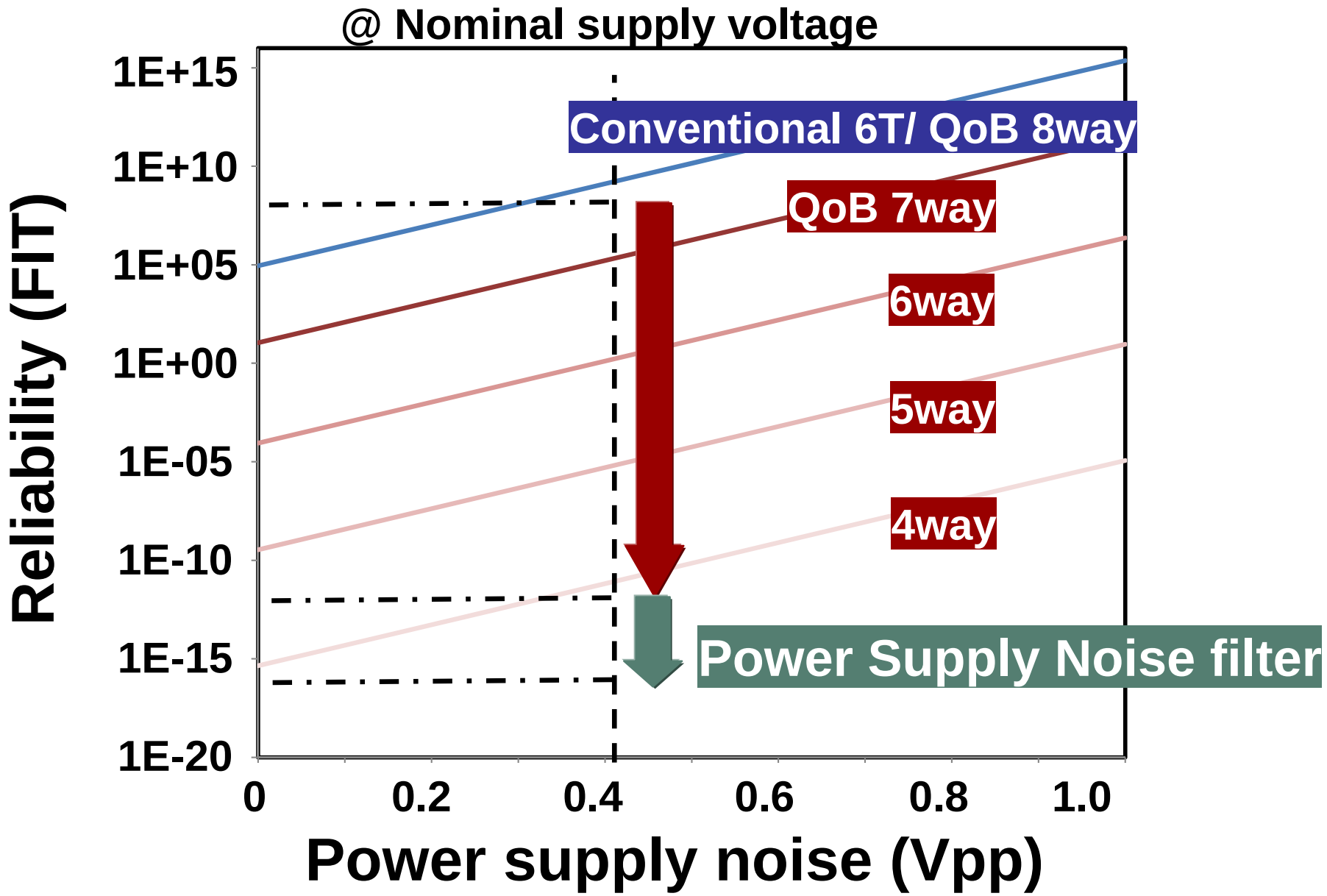
Irradiation board

Spallation neutron beam irradiates to the measurement board at RCNP. The measurement board includes 256-Kb SRAMs w/ and w/o triple wells.



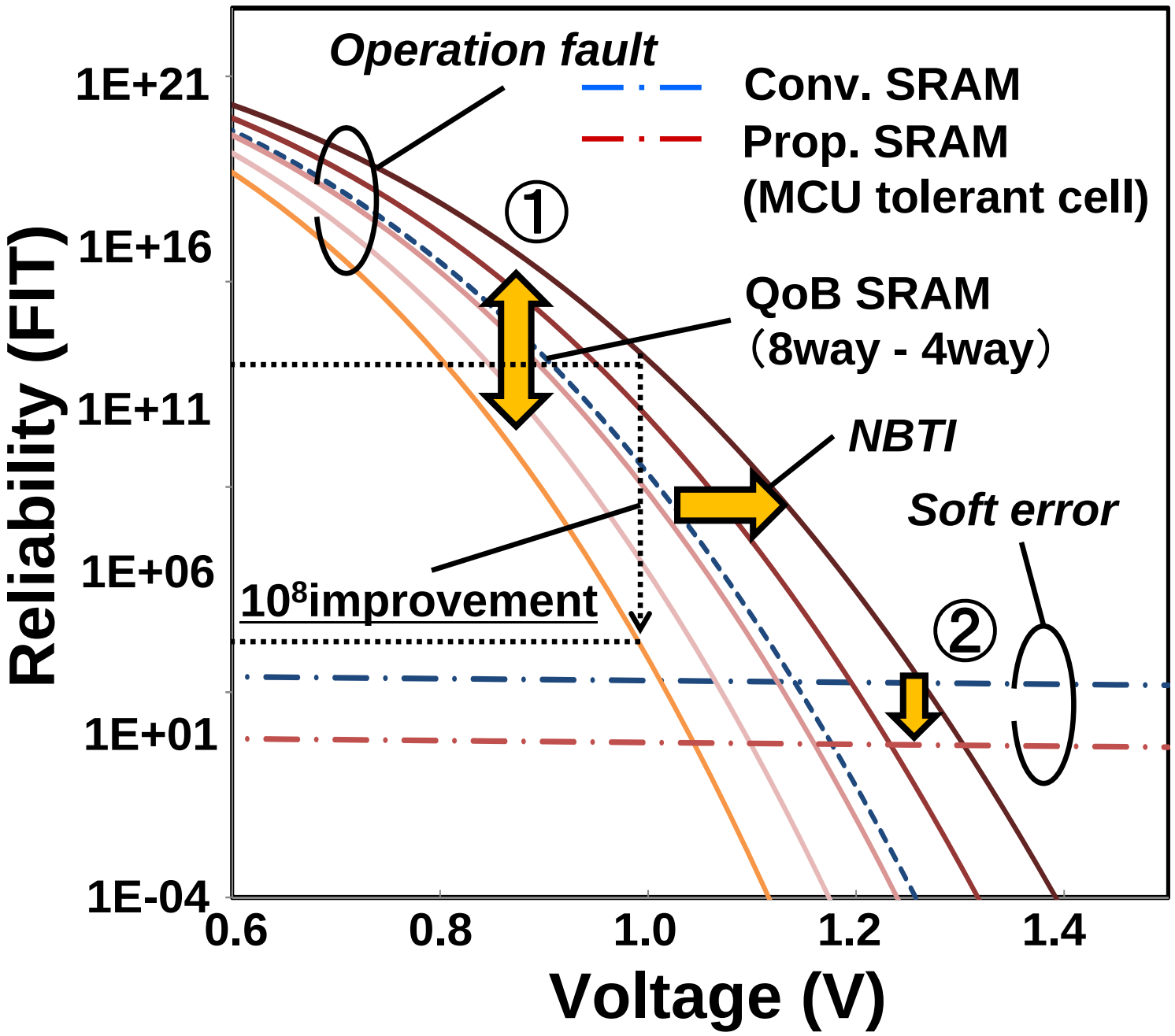
Horizontal MCU SER is improved by 67%–98%

Power supply noise tolerance



Dependability is improved by QoB cache and noise filter

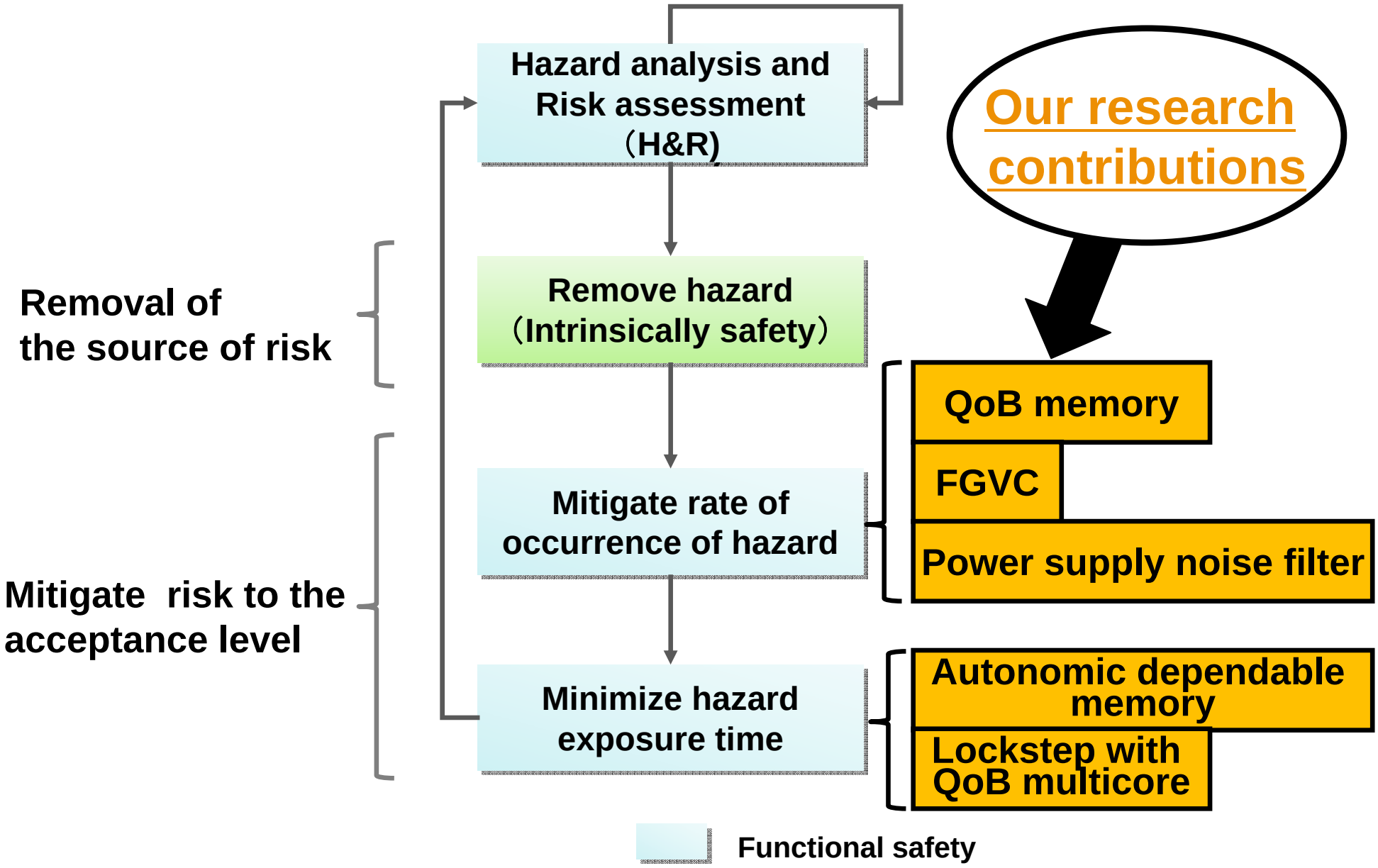
Reliability improvement evaluation



①Operation fault in low voltage region is saved by QoB cache.

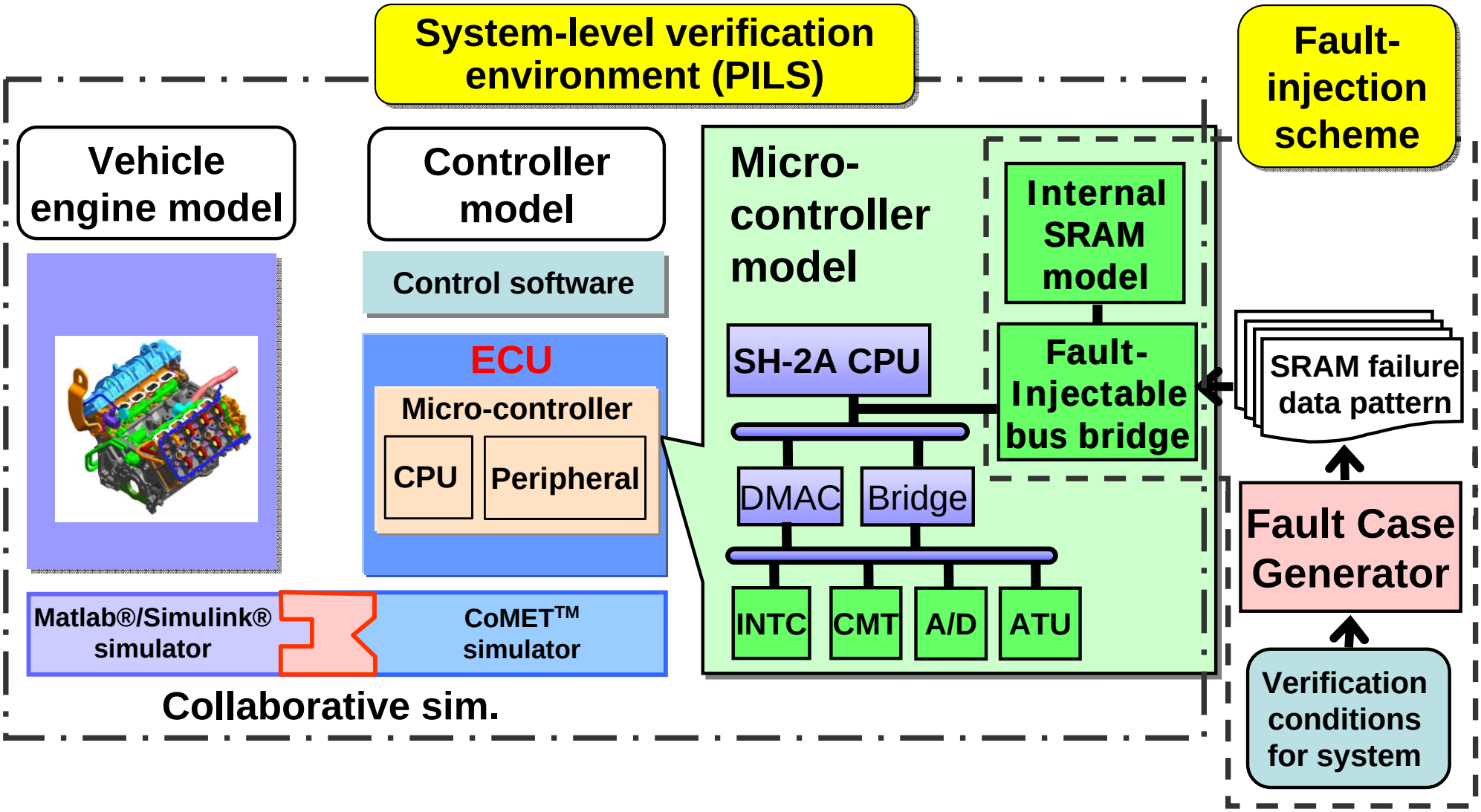
②Soft error in nominal voltage region is saved by MCU tolerant cell layout.

Functional safety



Source: ISO26262, Nikkei Electronics 2011.1.10, Fig.4, pp.50

Proposed Fault-Injection System (FIS)



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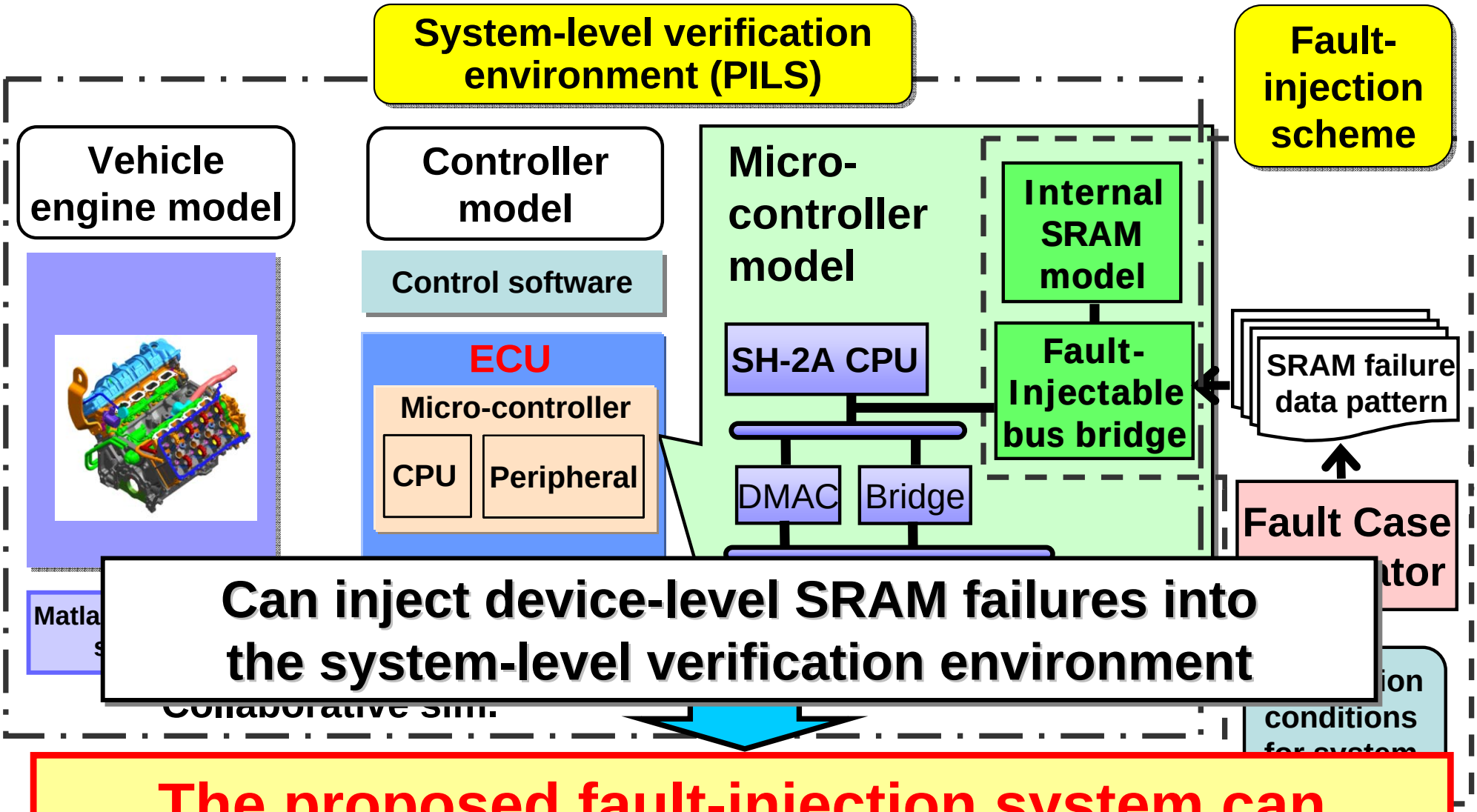
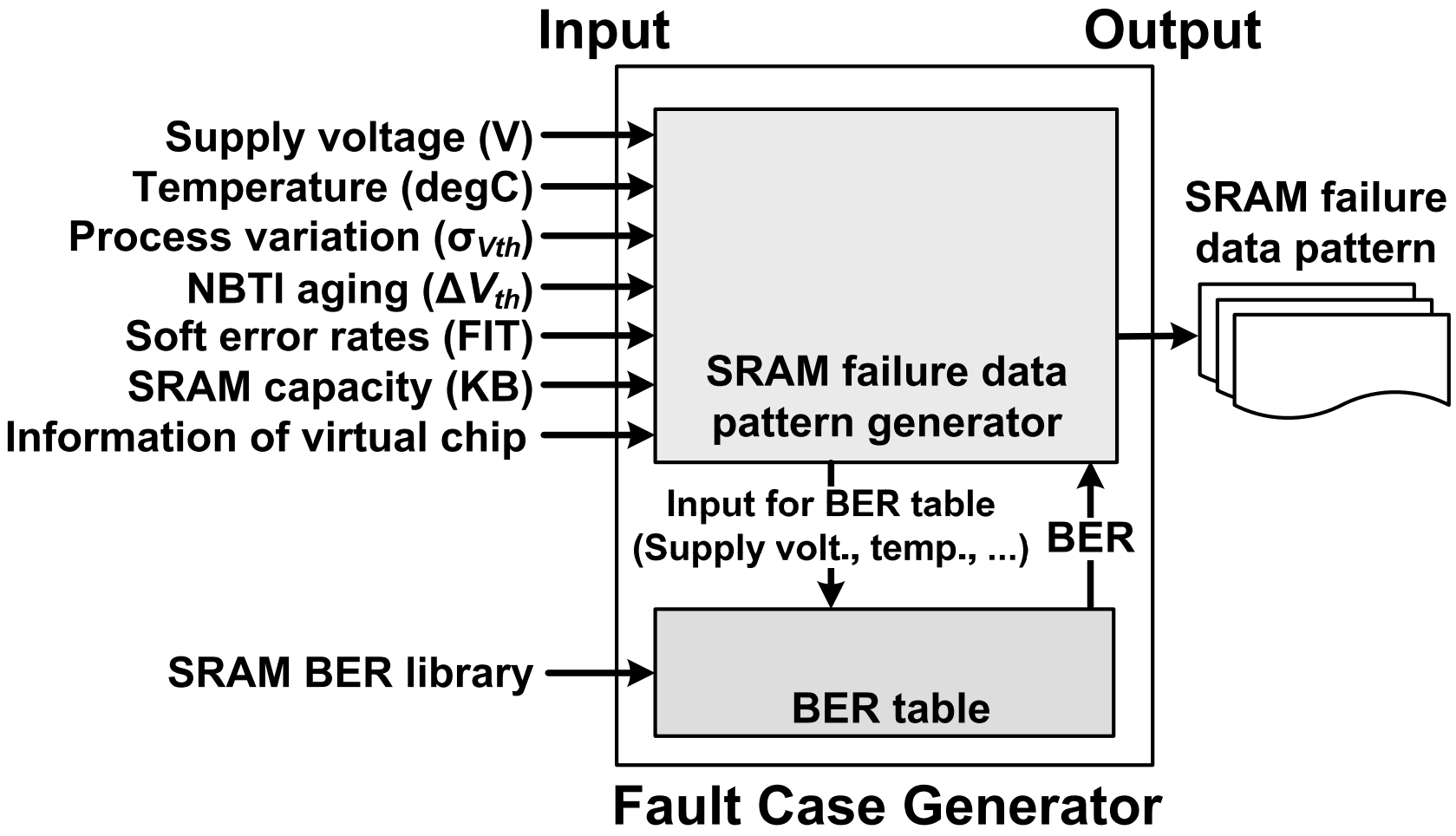


The proposed fault-injection system can evaluate <u>the impacts of SRAMs reliability on the operating stability of system</u>

Fault Case Generator (FCG)

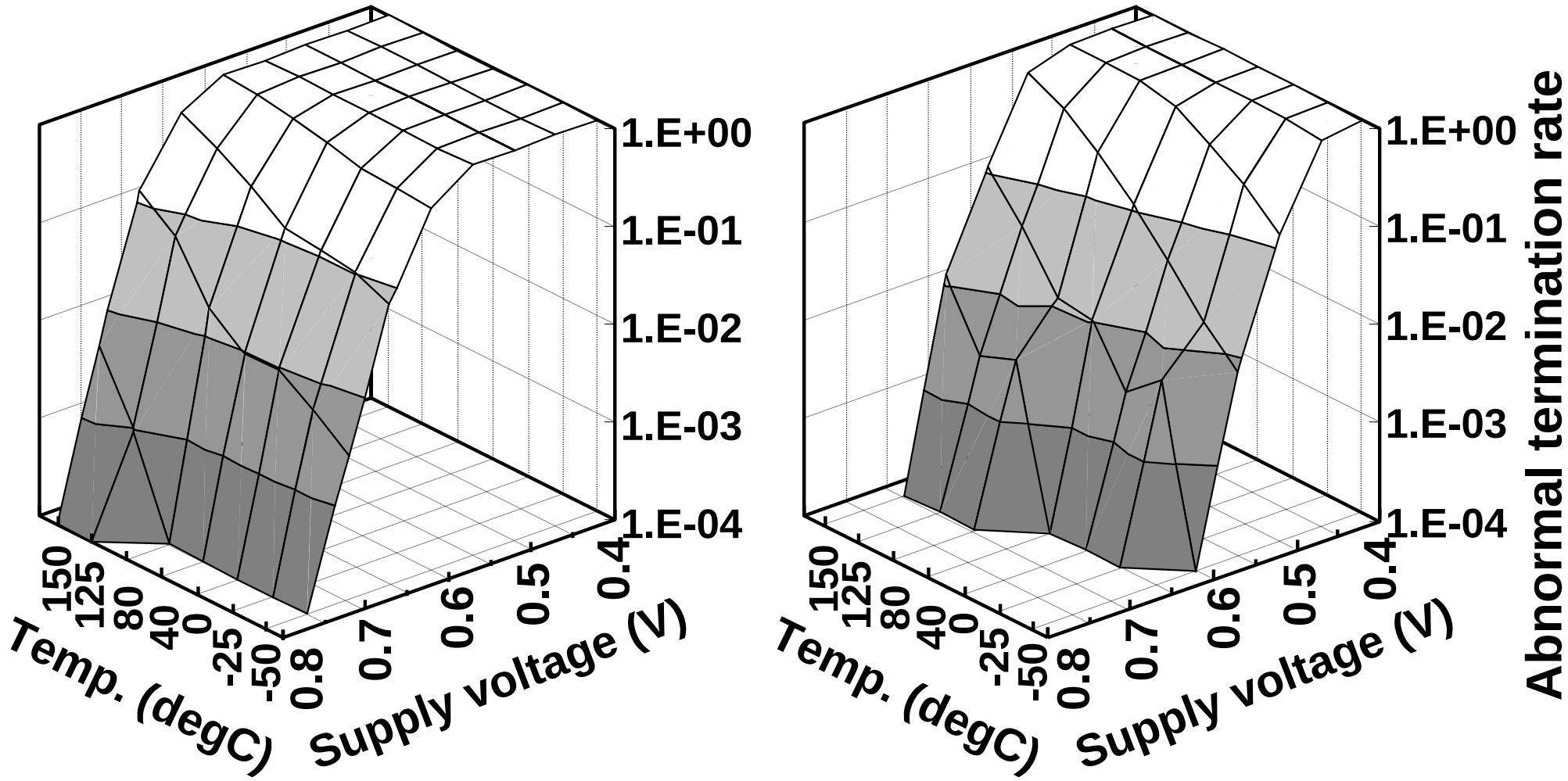


FCG can generates time-series SRAM failure data patterns correspond to arbitrary waveforms for the power supply noise and operating temperature, and device parameters

System-Level Evaluation Result

ECU System w/ 6T SRAM

ECU System w/ 7T/14T SRAM



ECU w/ 7T/14T SRAM improves the minimum op. voltage by 0.05–0.15 V

Summary

Question:

What is the definition of “dependability”?

Answer:

Reliability (FIT) against …

variation (mismatch),
aging (NBIT,HC) and RTN,
supply noise,
soft error

→ Reducing SRAM Vmin by autonomic controlled QoB and FGVC
→ Power noise monitor and filter
→ SER tolerant design (bitcell and system)