100M Dollar Lessons

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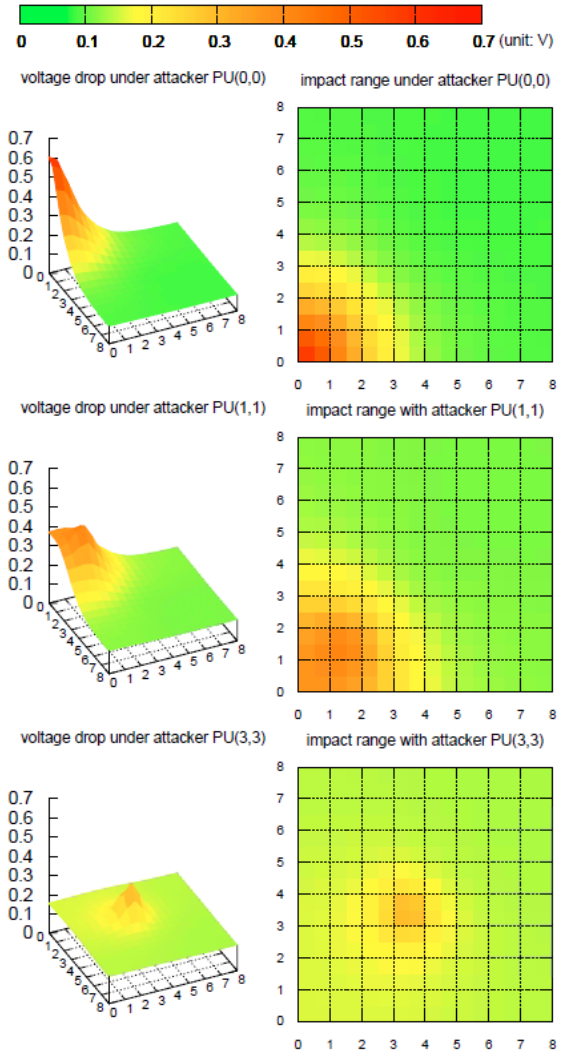
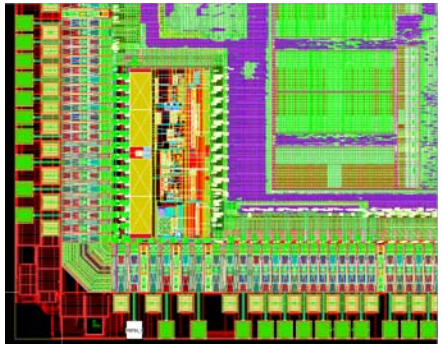
Ignorance of Reliability Hurts

- SDR baseband and application MPSoC
  - Four VLIW cores, one ARM core, over 20 peripherals
  - Less than 1W on average
- Yield is very low
- We find this is caused by on-chip power grid noise
- We are the victim of this new reliability issue
  - Tools from all major EDA companies fail to detect such problem
  - No similar report in literature at the time
- Cost
  - 15 engineers and 11 months
  - Expensive chip re-spin
  - Delayed contract
  - Investor confidence



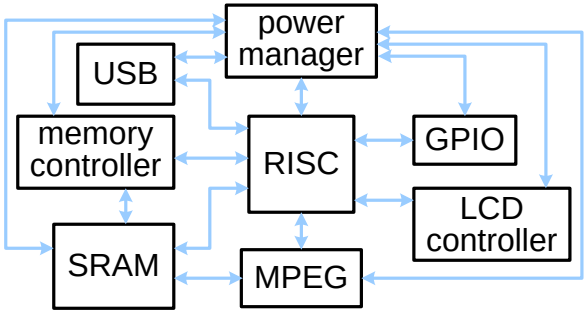
Network-on-Chip Helps

- Performance
  - Cooperation among functional units and chips
  - Communication latency
- Power consumption
  - Significant dynamic power used by communications
  - Considerable leakage of interconnect drivers and buffers
- Scalability
- New functionalities for
  - Online testing
  - Dynamic reconfiguration
  - …

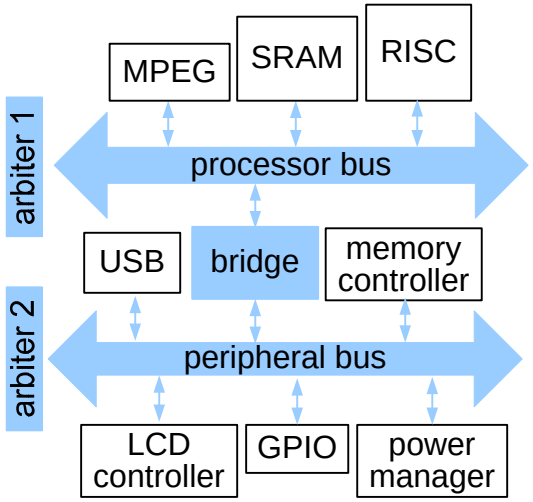


On-Chip Communication Architectures

- Ad hoc interconnect networks
  - Dedicated point-to-point interconnects
  - Design is intuitive and simple
  - Not cost-effective for complex systems

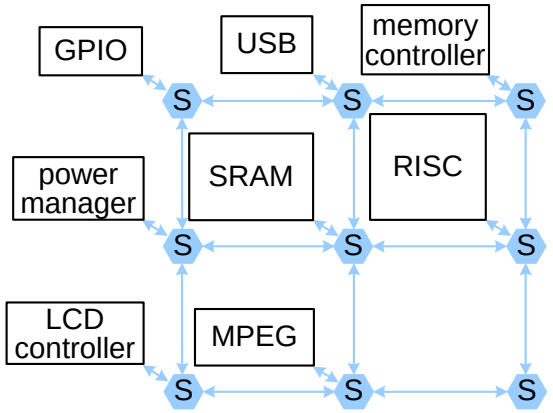


- On-chip buses
  - AMBA, CoreConnect, µNetwork, Wishbone …
  - Shared media communication architectures
  - Mature technology
  - Limited throughput and high power consumption

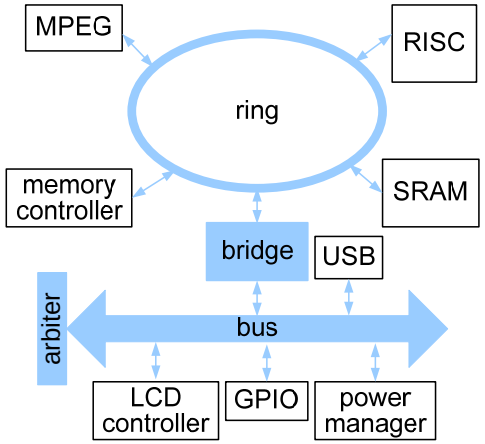


On-Chip Communication Architectures

- Network-on-chip
  - Inspired by multi-computer and multi-processor networks
  - Switching and routing techniques
  - Regular and irregular topologies
  - High-throughput, scalable
  - Large overhead



- Hybrid on-chip networks
  - Use a combination of the other three types
  - Very flexible
  - Complex design and analysis



Thanks!