Panel Session 3: Architecture & Circuit

■ Moderator

M. Yoshimoto (Kobe Univ.)

■ Invited Panelists

K.Osada（Hitachi）:H/W for Functional Safety

K.Anami（ISIT）:System Level Verification

■ JST/CREST DVLSI Panelists

N.Yamasaki（Keio Univ.）: Embedded RT System

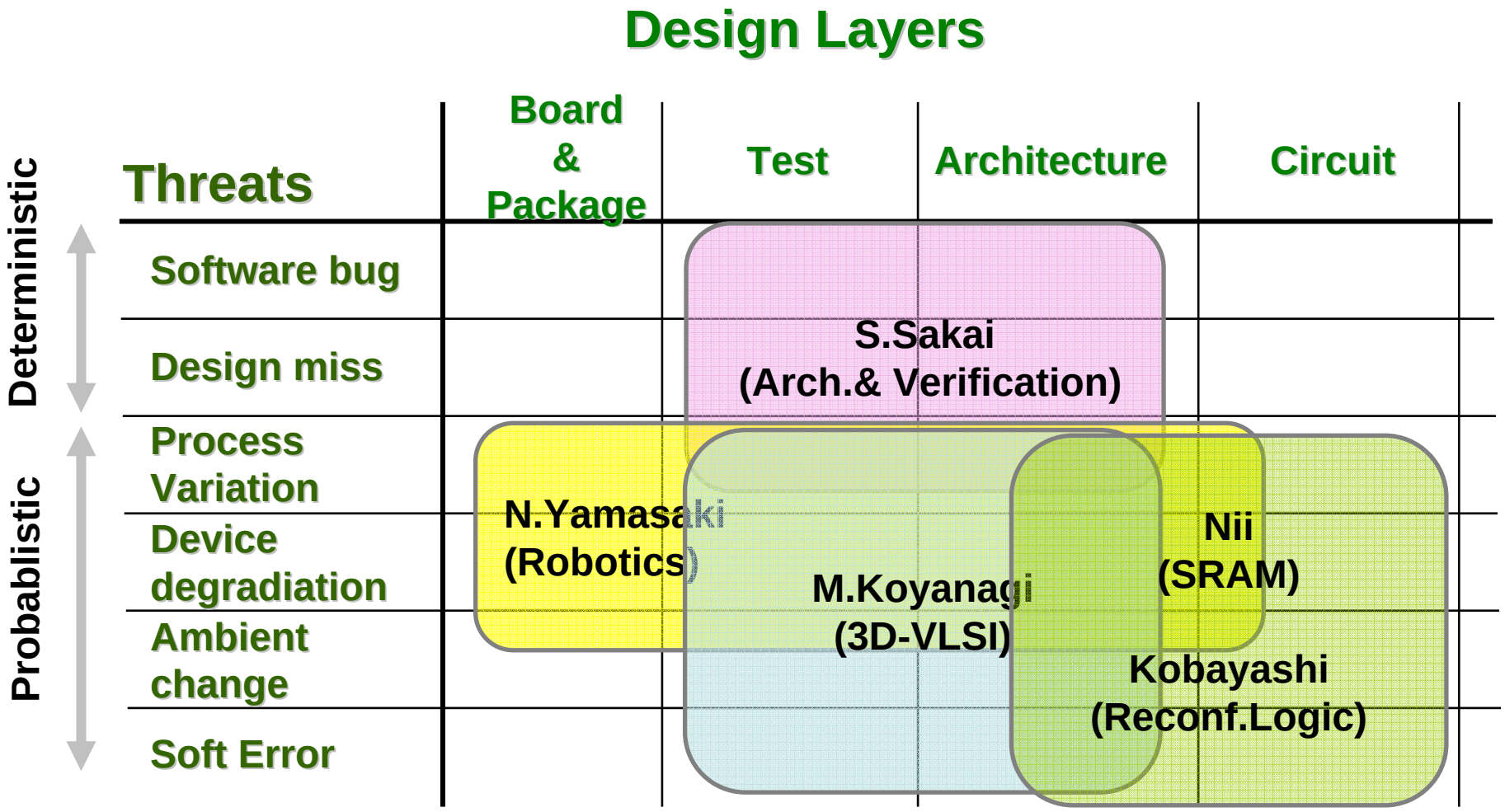
S.Sakai（Univ. of Tokyo）: Architecture/Verification

M.Koyanagi（Tohoku Univ.）: 3D-VLSI

K.Kobayashi（Kyoto Inst. Tech.）: Reconfigurable Logic

K.Nii（Renesas）: SRAM

Research area covered by JST/CREST panelists



Discussion Subjects (cont'd)

- 「ディペンダビリティ指標」とは何か。

How can we define indices for dependability of VLSIs and their application systems?

Please demonstrate the most convenient indices which expresses contributions of your research.

- 「ディペンダビリティ指標」を向上させるための提案技術。

What are proposed architectures and/or circuits to improve indices?

- 提案技術はディペンダビリティ指標をどのように向上させるのか。

How can this program improve them and benchmark competing world's research efforts?

Discussion Subjects

・アーキテクチャ、回路の提案をどうシステムのディペンダビリティ評価までつなげるのか？

How do we estimate dependability improvement of target system based on proposed techniques?

・ISO26262、IEC61508の規定する機能安全水準に照らして、おのおのの研究がどんな意味を持つのか。

How can this program meets functional safety standards in ISO26262 and IEC61508 ?

Panel Session 3: Discussion Summary

	Research Area	Proposed Techniques	Index	Remarks
Yamazaki	Embedded system	SoC-SiP-Board co-design		SIL-3
		RTOS-Processor-Communication co-design		
Sakai	Architecture & Verification	Best effort design		
		Run time recovery		
Koyanagi	3D-VLSI	3D DfT Architecture. Redundancy,	FIT	ASIL-C/80FIT
		Self -repair scheme		
Kobayashi	Logic/FPGA	Reconfigurable Array	?	
		DARA	MTTF	
		BCDMR FF	FIT/Mbit	
Nii	SRAM	Autonomous dependable SRAM	FIT	
		DMR with QoB MultiCore	FIT with small OVH	
		Virtual-HILS with fault injection		

Panel Session 3: My Impression

System level evaluation & Methodology
(Reliability, Availability, Functional Safety, Security, Maintenancibility)

Overhead reduction
(Performance, Power, Cost etc)

Innevitable for Practical utilization!