Dependable Memory Techniques for Highly Reliable VLSI System

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Dependability degradation factor

<u>Dependability</u> <u>degradation factor</u>

 $V_{\rm th}$ variation

NBTI, temperature fluctuation

Power supply noise

Soft error

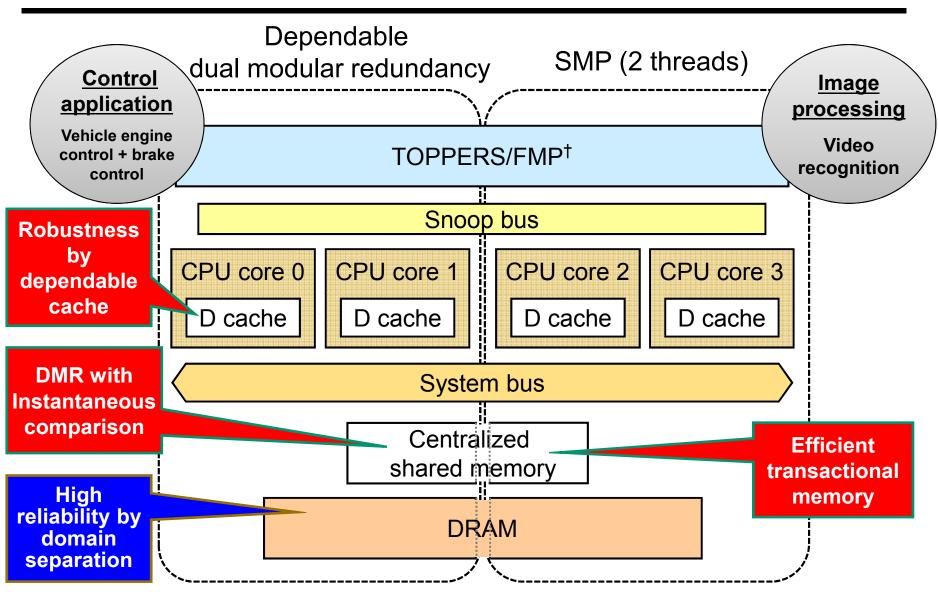
Improvement / tolerant technique

- QoB Cache
- FGVC memory (with BIST)
- Lockstep with QoB multicore
- Power supply noise filter
- Autonomic memory with ODM
- Lockstep with QoB multicore
- Soft error tolerant memory cell
- Lockstep with QoB multicore

QoB: Quality of Bit

FGVC: Fine-Grain Voltage Control

Dependable QoB multicore processor system



[†] TOPPERS/FMP: new generation kernels - to provide support for multi-core processors. Both symmetric and asymmetric configurations are supported by TOPPERS project.

Instantaneous Block data comparison (QoB) for Dual Modular Redundancy

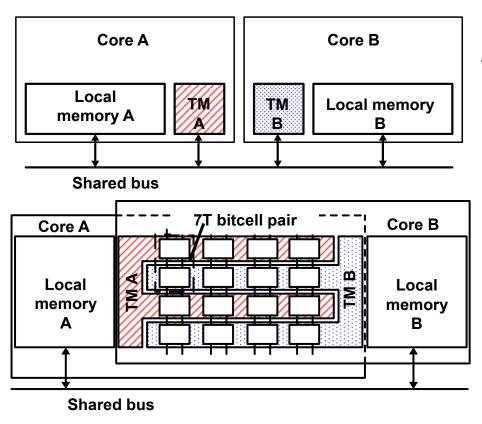
BL N_△ $\mathsf{BL}_{\mathtt{A}}$ Variation in transistors is a critical issue for a reliability of LSI **Bitcell A** ⇒DMR is one way to improve the reliability. WL_{Δ} **Comparison SRAM VDD**_{*} Block A Result CORE (match / CORE miscompare) Data B Block B Data B **CTRL VDD** L1 L1 Result 7T DMR (Dual Modular) bitcell \mathbf{WL}_{B} Redundancy) pair Bitcell B BL_N_B **BL**_B Proposed SRAM is useful for DMR, When different data are stored, a it realizes high-speed & low-power data comparison. supply current flows through the 1.25 connecting pMOSes Normalized power 0.75 0.5 0.25 **Detecting miscompare bitcell pair** by the supply line voltage In the proposed SRAM, 8-kb data can 0.86 93.4% be compared in 130ns. 92.3% The proposed scheme reduces power consumption by 0.07 93.4% and 92.3% compared with EXOR comparison 0 comparison EXOR Proposed comparison

CRC: Cyclic Redundancy Check

circuit and CRC comparison circuit

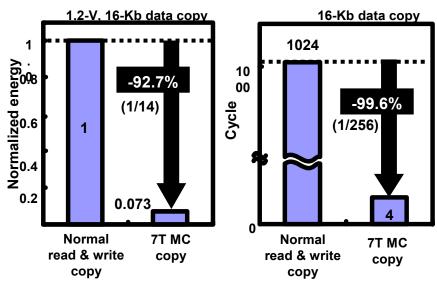
Instantaneous Block data copy (QoB) for Transaction memory

Transaction Memory at multicore processor



(a) general case and (b) copiable 7T SRAM architecture for transactional memory

Apply to instantaneous data copy scheme.

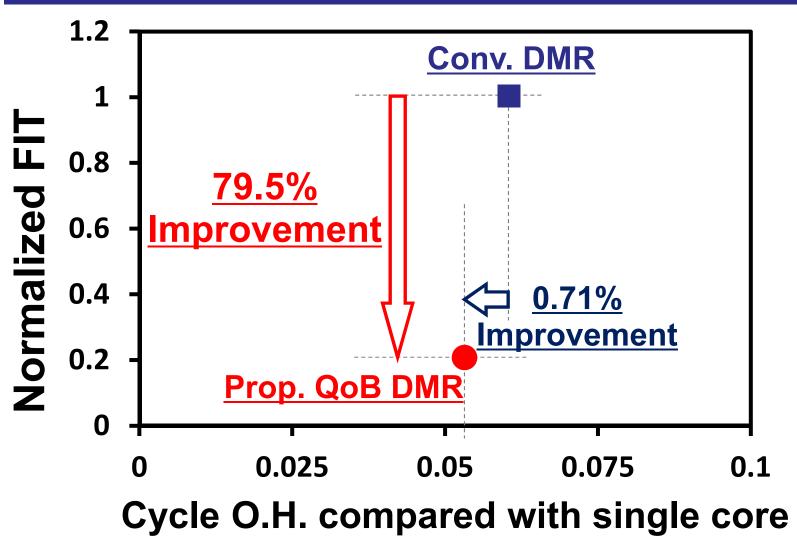


In transaction memory, high speed recovery without shared bus is realized.

Data copy energy is saved 92.7%. Copy cycle is saved by 99.6%.

FIT and cycle O.H. improvement of QoB DMR

At higher SRAM FIT (low op. voltage) situation



FIT and cycle O.H. improvement of QoB DMR

At lower SRAM FIT (nominal op. voltage) situation

