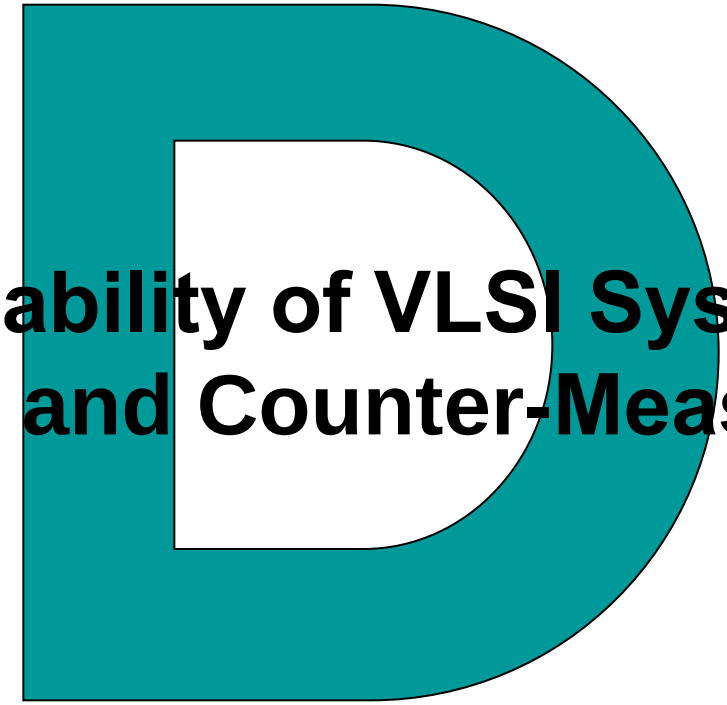
Kyutech
Kyushu Institute of Technology

JST International Symposium on Dependable VLSI Systems 2013
Tokyo, Japan
December 6-7, 2013



"Dependability of VLSI Systems– Threats and Counter-Measures"

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The "Dependable VLSI Systems" is a collaborative university-industry research program funded by Japan Science and Technology Agency under the CREST* framework.

Program term: FY2007~2014

- In its 7th year of the 8-year term

CREST: http://www.jst.go.jp/kisoken/crest/en/index.html

The term 'VLSI Systems' refers to systems that use VLSIs as key components, as well as complex VLSIs as systems.

Rationale for research in DVLSI

VLSI: Is the component key to systems of all kinds. Its dependability is at the foundation of systems dependability.

Problems: Threats against VLSI systems are actually increasingly, and possible consequences of failures are increasingly more devastating.

Threats arising from miniaturization

- Variations in dimensions, shapes, doping densities,
- Decrease in S/N ratio (radiation, EMI, fixed and floating charges),
- Aggravating wear/fatigue phenomena (NBTI, hot carriers, electro-migration).

Threats arising from increased complexity

- Higher levels of integration,
- Enhanced functionality (id, encryption,---)
- Multiple- Many-core architecture, multi-thread operation,
- Heterogeneous integration
  - Analog, digital, nonvolatile, network, sensors, actuators, etc.

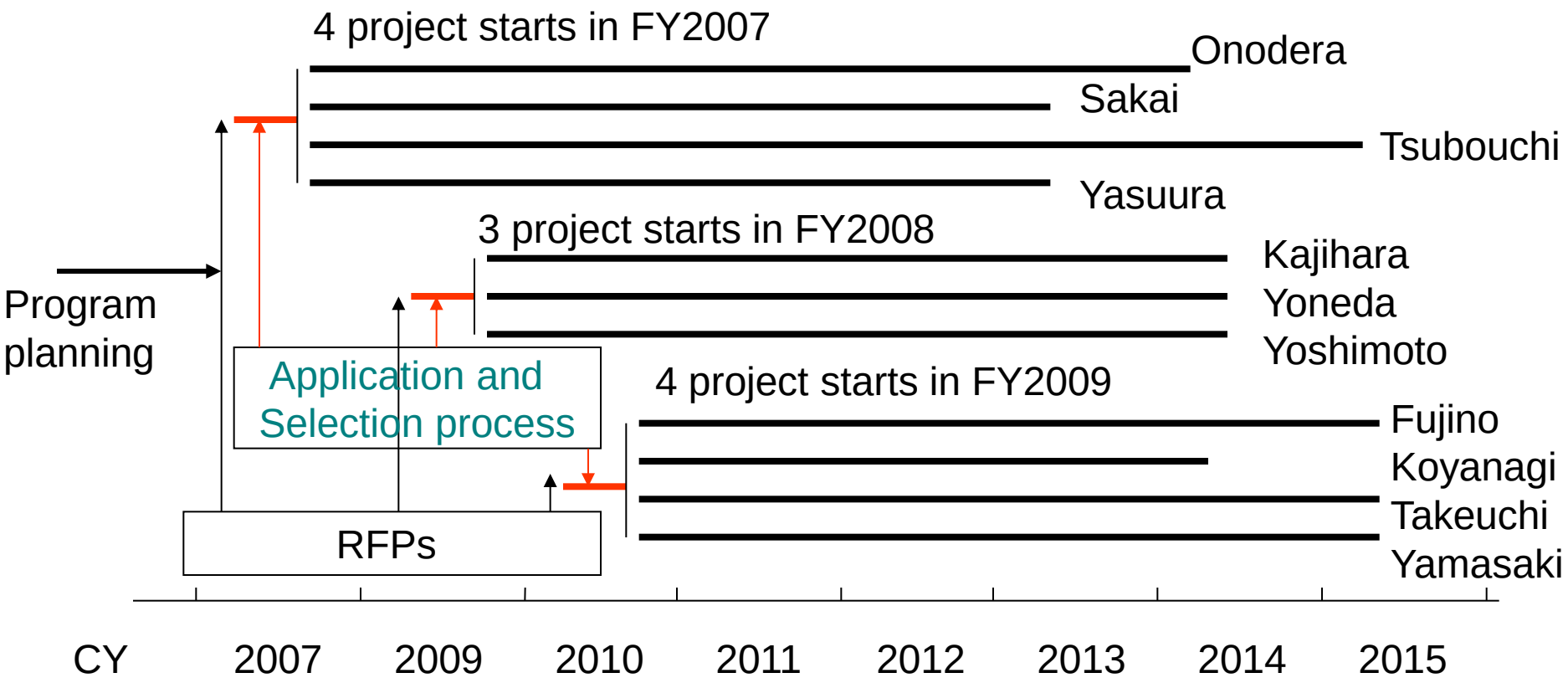
Missions of the DVLSI Program:

1. Contain Rising Threats within VLSIs (Components Supposed to be Most Dependable) by Design and/or Testing,

2. Provide New Functionalities in VLSI which Improve Dependability at Systems Level,
   - VLSI for 'Functional Dependability'

3. Provide Means to Evaluate/Measure Dependability

Selection and Terms of the DVLSI Projects



Program Term: 2007- 2015

A Brief Preview of DVLSI 2013

Friday

Session 1 Connectivity in Wireless Communications and 3D Integration

Session 2 Mixed Topics: Resilient Systems, SRAMs for Robust Systems, Testing for Reliability

Saturday

Session 3 Soft Error-Tolerant Design, Variability-Aware Design

Session 4 Real Time Response

Session 5 Mixed Topics: Automotive, Tamper Resistance, Combined Test and Debugging

Panel Discussions What is expected for dependability?

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Thanks to Kyushu Institute of Technology for Sponsoring

九州工業大学には本シンポジウムの共催支援を感謝申し上げます。

Thanks to the Organizing Committee Members of this Symposium:

Chair: Seiji Kajihara (Kyushu Institute of Technology)
Secretary: Satoshi Otake (Oita University)
Members: Masahiko Yoshimoto (Kobe University)
Tomohiro Yodena (National Institute of Informatics)
Hiroshi Kawaguchi (Kobe University)

本シンポジウムのプログラム委員会に感謝申し上げます。
梶原先生、大竹先生、吉本先生、米田先生、川口先生

Thanks to Invited Speakers:

Meng-Fan (Marvin) Chang, National Tsing Hua University
Valentin Gheorghiu, Qualcomm Standards and Industry Organizations
Krishnendu Chakrabarty, Duke University
Mehdi B. Tahoori, Karlsruhe Institute of Technology
Wilfried Steiner, TTTech Computertechnik AG
Camille Vuillaume, ETAS K.K.
Roger Barth, Micron Technology

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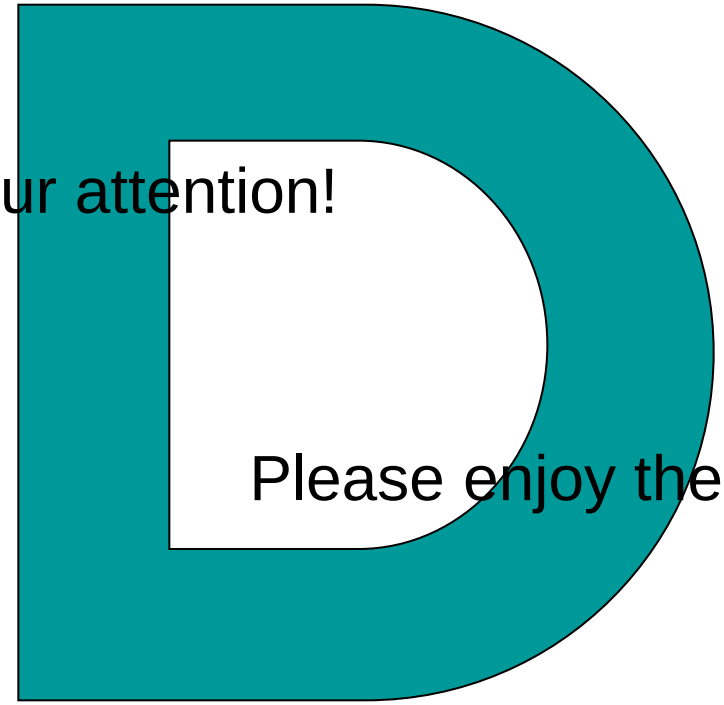
JSTの本プログラム関係者に感謝申し上げます。

Thank you for your attention!



Please enjoy the conference!

For more details about DVLSI, visit the website:
http://www.dvlsi.jst.go.jp/
http://www.dvlsi.jst.go.jp/english/index.html