Soft-error and Variability Resilience in Dependable VLSI Platform

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Outline: Soft-error and Variability Resilience

- Background
- Overview: Dependable VLSI Platform
- Circuit-level Resilience
  - Soft-error tolerant FF
  - Variation tolerant FF
  - Variability compensation by localized body-biasing
- Architecture-level Soft-error Resilience by Reconfigurable Array
- Platform SOC and C-based Design Tools
- Summary
Background:
Overall Design Technology Challenges (ITRS2011)

- Design productivity
- Power consumption
- **Manufacturability**
  - Performance/power variability, device parameter variability, lithography limitations
- Interference
- Reliability and resilience
  - Logic/circuit/physical: MTTF-aware design, built-in-self-repair, soft-error correction
Dependable VLSI Platform using Robust Fabrics

- **Target:** Resolving the challenges in **Manufacturability, Variability, Aging, Soft errors, NRE-cost explosion**
- **Method:** Collaborative researches for Layout/Circuit/Architecture/Mapping
  - Layout: Robust structure for enhanced manufacturability
  - Circuit: Adaptive performance tuning
  - Architecture: Adaptive redundancy in reconfigurable architecture
  - Mapping: dependability-aware HLS and mapping from C
- **Goal:** Dependability-aware VLSI Platform

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Dependable VLSI Platform

**Dependable Processor**

**DMAC**

**SRAM (Local Memory)**

**WISHBONE**

**Direct I/O**

**Ext. I/O**

**Reliability-aware Mapping (Controller, etc.)**

**Application in C**

- Digital Filter (FIR, IIR), CRC, FEC (LDPC, Viterbi), Cipher (AES),

**Reliability & Area aware Mapping (I/Os, etc.)**

**Area-effective Mapping (Datapath etc.)**

**Reliability – Area Tradeoff**

- Reliability: Max
- Reliability: Regular
- Reliability: High
- Area: Small
- Area: Min.
Target Applications

Application
- Streaming
- Automotive
- Space/Aero
- Base Station
- Storage

Dependability Aspects
- Cost Performance
- Low Power
- Programmability
- Manufacturability
- Soft Error Resilience

Dependable VLSI Platform
- Robust Fabric
- Flexible Reliability Reconfigurable Array
- Reliability-aware Mapping
- Dependable Processor

Proposed Key Technology

Conventional Technology
- Cell Library
- FPGA
- Place and Route
- Embedded Processor
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Soft-error Tolerant FF: BCDMR FF

- Improvement of BISER
  - Eliminate vulnerability to SET at the master C-element.

**Data Redundancy in 2 latches and c-element**

![Diagram of BISER FF and BCDMR FF](image)

- BCDMR: Furuta, et.al., VLSI Ckt., 2010.
**Measured Resilience for Soft Errors**

- **Neutron irradiation test for 50 min.**
  - No error is observed in 202,000 BCDMR FFs (65nm)
  - At least 260x stronger than conventional FFs

- **α-particle irradiation test for 5 min.**
  - No error is observed in operating condition

<table>
<thead>
<tr>
<th>Clock Freq.[MHz]</th>
<th>100</th>
<th>300</th>
<th>800</th>
<th>1000</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>well</strong> twin</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td><strong>well</strong> triple</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Conventional FF: #errors:260
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Variation Tolerant FF

- Vulnerability of D-FF Timing Characteristics under WID Random Variation
  - Simulated D-to-Q Delay and Setup Time at the SS and SKEW Corners

<table>
<thead>
<tr>
<th>Corner</th>
<th>D-to-Q Delay [rise/fall]</th>
<th>Setup Time [rise/fall]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SS</td>
<td>1.00/1.00</td>
<td>1.00/1.00</td>
</tr>
<tr>
<td>SKEW</td>
<td>0.91/0.95</td>
<td>1.18/1.88</td>
</tr>
</tbody>
</table>

- Simulated D-to-Q Delay and Setup Time at the SS and SKEW Corners
  - Due to the skewed delay characteristics between the latching loop and the clock drivers

Sunagawa, et.al. SOCC2009
Variation Tolerant FF

- Variation Tolerant FF Design
  - Enhanced Clock Driver
  - TSPC (Single Phase Clock)

Variation Tolerant FF Design

Enhanced Clock Driver

TSPC (Single Phase Clock)

Clock Driver

Enhanced

Standard

TSPC

DFF Test Structure

Maximum Operating Frequency for 3240 FFs in 65nm
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Variability Compensation by Localized Body Biasing

- **Features**
  - Variability compensation by fine grain (~0.1mm²) adaptive body biasing
  - “SS”, “SF”, “FS” corner performance can be compensated to “Typical”
  - Area overhead less than 3%

- **Developed IPs**
  - All-digital pMOS/nMOS monitors
  - Cell-base-designed body biasing circuits

- **Other Features**
  - WID as well as D2D variability compensation
  - Compatibility with Cell-base design
Variability Compensation by Localized Body Biasing

- **Performance Compensation in Corner Chips (SS, SF, FS, FF, TT) at Vdd=0.7V**

- **nMOS/pMOS FET Monitor**
- **Cell-based Design**
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Reconfigurable Architecture with Flexible Reliability

Course/Fine-Grained Reconfigurable Architecture for Flexible Reliability
Reconfigurable Cluster Array Structure

3 reliability levels

<table>
<thead>
<tr>
<th>Level</th>
<th>Redundancy</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Config.</td>
<td>EM</td>
</tr>
<tr>
<td>TMR</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>SMS</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>SMM</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Combination of Coarse-grained and Fine-grained Elements

Control

Datapath

Application mapping

Fine-grained element (LUT cluster)

Dependable VLSI platform SoC

Coarse-grained element (ALU cluster)
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Dependable VLSI Platform SoC and C-based Design Tools

- **Dependable VLSI Platform Hardware**
  - Flexible Reliability Reconfigurable Array (FRRARY)
  - Reliable Processor (DARA)

- **Dependable VLSI Platform Software**
  - C-based High-Level Synthesis
  - Reliability-aware Mapping

Design Tools

- Dependable VLSI Platform Hardware
  - Flexible Reliability Reconfigurable Array (FRRARY)
  - Reliable Processor (DARA)

- Dependable VLSI Platform Software
  - C-based High-Level Synthesis
  - Reliability-aware Mapping

**Evaluation system**

- **Dependable VLSI Platform SoC**
  - 65nm CMOS
  - 4.2mm x 4.2mm
  - #clusters:
    - ALU: 26
    - Memory: 6
    - LUT: 80

- **Design Tools**
  - Camera In
  - Display
Dependable VLSI Platform SoC and C-based Design Tools

- ANSI-C
  - Partitioning for acceleration and program translation
- C program for processor
  - Behavioral synthesis (CWB)
  - Data flow graph (DFG)
  - Placement
  - Routing
- Machine code program
- Configuration data
- Reliable processor (DARA)
- Reconfigurable cluster array (FRRAry)
- Dependable VLSI platform

- C-based Design Flow
- Area-Reliability Trade-off by Partial TMR
α particle irradiation test
Target: Resolving the challenges in **Manufacturability, Variability, Aging, Soft errors, NRE-cost explosion**

**Solutions**
- **Fabrics**: Soft-error and variation tolerant FFs
- **Circuit**: Adaptive performance tuning by localized body biasing
- **Architecture**: Adaptive redundancy in reconfigurable architecture
- **Mapping**: Dependability-aware HLS and mapping from C

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**Application in C**
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- Reliability & Area aware Mapping (I/Os, etc.)

**Dependable VLSI Platform**
- **DMAC**
- **SRAM** (Local Memory)
- **External I/Fs**
- **Direct I/O**
- **Ext. I/O**
- **Reconfigurable Cluster Array (FRRARY)**
- **Reconfigurable Array I/F**
- **WISHBONE**
- **Dependable Processor**

**Reliability – Area Tradeoff**
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