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Development of Dependable Wireless System and Device

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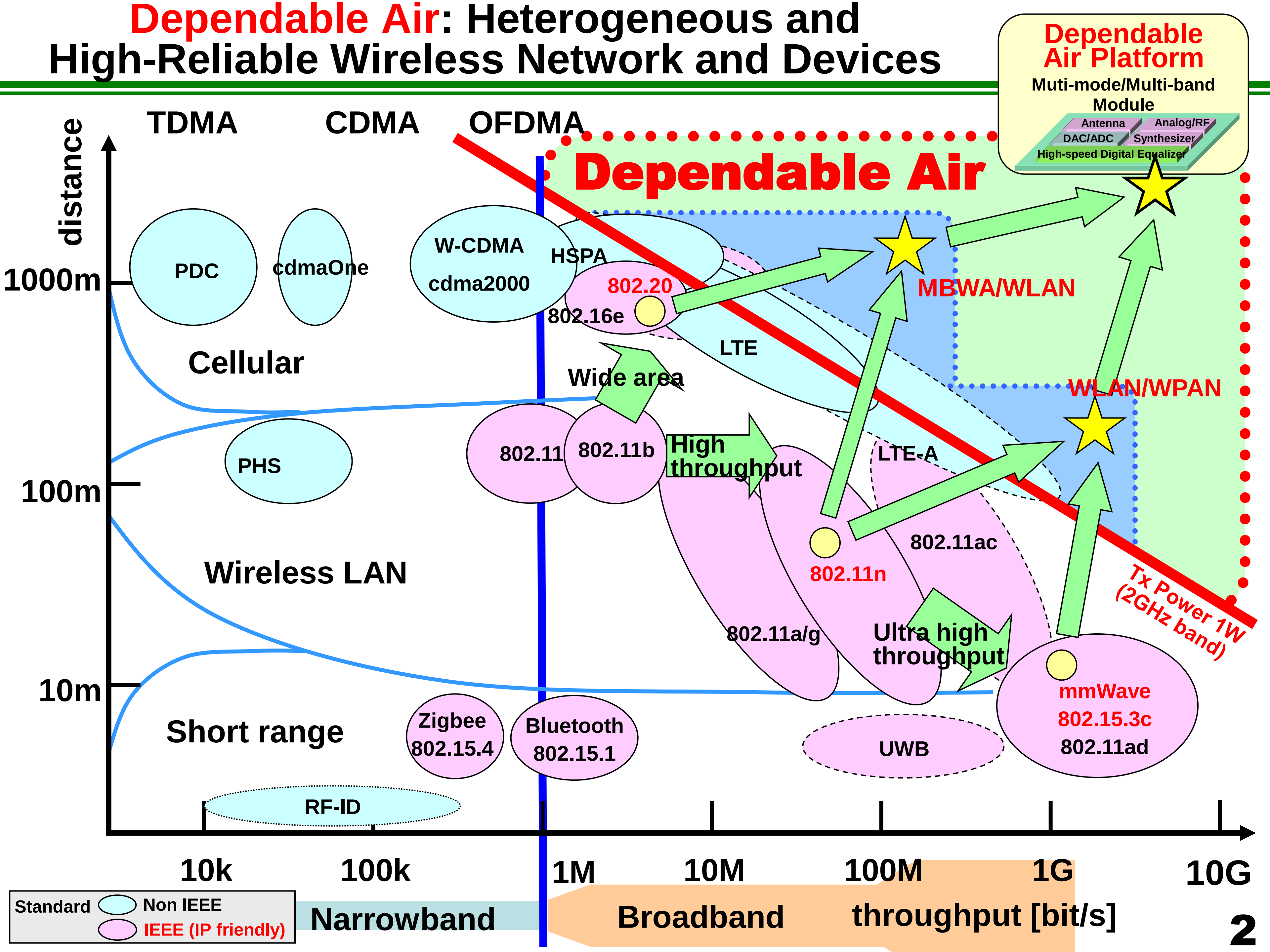
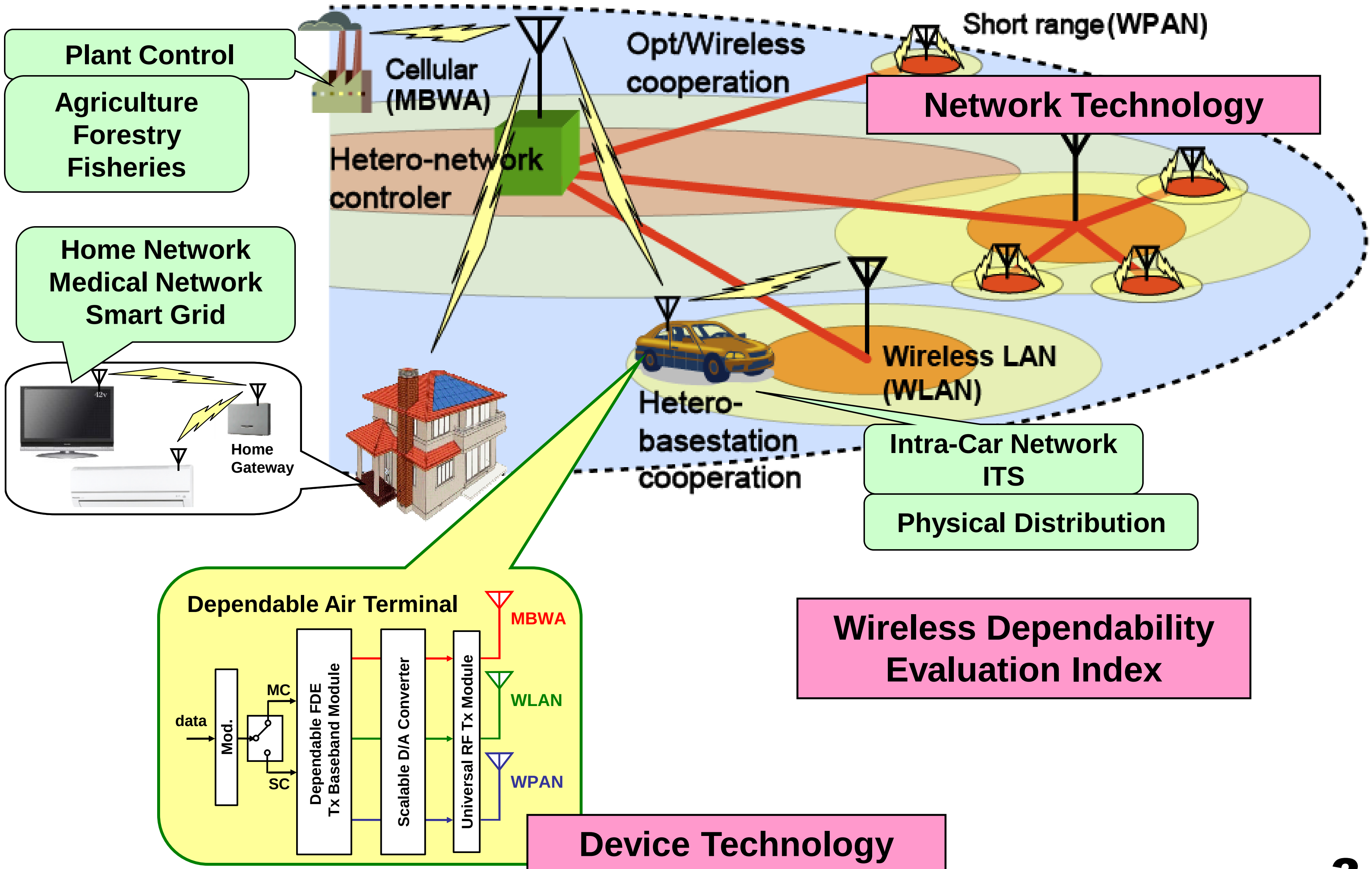
SoftBank Mobile Corp. *etc.*

Dependable Air: Heterogeneous and High-Reliable Wireless Network and Devices

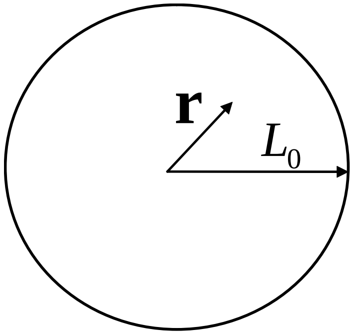


Summarize the R&D Areas for Dependable Air



Wireless Dependability Evaluation Index

Wireless Dependability Index *F*



Communication control area: Cell radius L_0, Spread S

Definition

Total throughput index *F* of communication control area

$$F = \oint_S R(\mathbf{r})d\mathbf{r} \quad (1)$$

Throughput of point r

Simplification

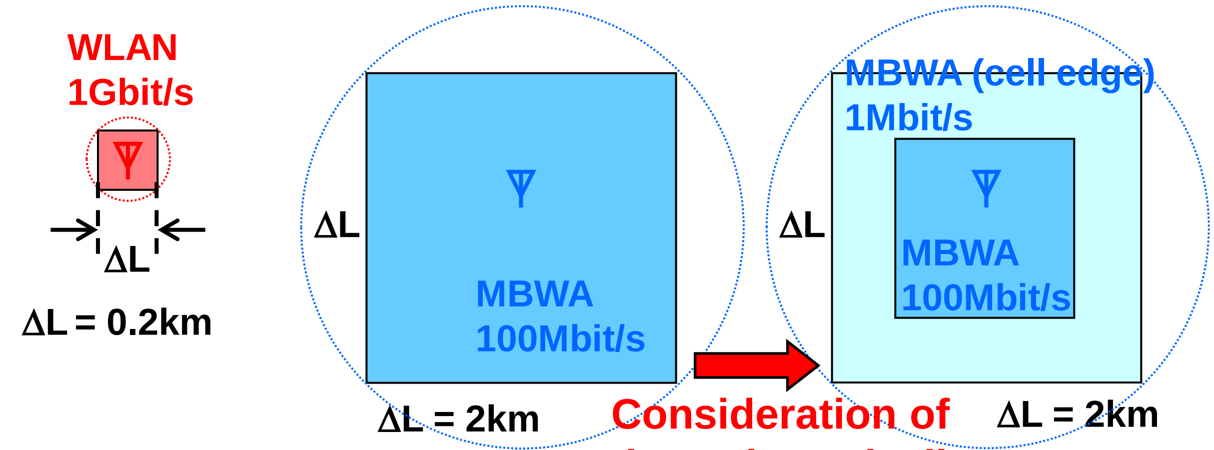
$$F = S \cdot R_{eff} \quad (2)$$

$$R_{eff} = \sqrt{R_{max} R_{min}}$$

R_{max}: Max R(r)
R_{min}: Min R(r)

[1] K. Tsubouchi et al., IEICE Trans. Commun., J95-C(12), Dec. 2012.
[2] T. Takagi et al., GSMM2013.

WLAN single cell	MBWA single cell	MBWA multi cell
F = 40	F = 400	F = 40



Consideration of throughput decline at the cell edge

Conventional standards

Single system:
Max *F* = 30

	L^2	R_{max}	R_{min}	F
HSPA	2^2	14	0.14	5.6
LTE	2^2	75	0.75	30
WiMAX	2^2	40	0.40	16
IEEE802.11n	0.2^2	450	4.5	1.8
IEEE802.11ac	0.02^2	6930*	69.3	0.277
IEEE802.11ad	0.02^2	7000*	70	0.28

Wireless Dependability Index *F*: Hetero-Network

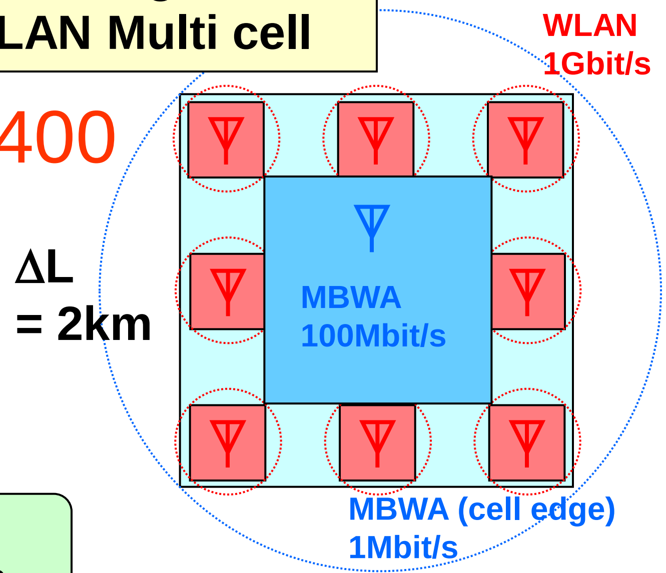
Dependable Air:
***F* improves by using combinations of hetero-networks.**

Single cell

$$F = S\sqrt{R_{\max} \cdot R_{\min}} \quad (3)$$

MBWA Single cell + WLAN Multi cell

F = 400



Hetero-cell

$$F_{h2} = S\sqrt{R_{2,\max}\sqrt{R_{1,\max} \cdot R_{1,\min}}} \quad (4)$$

- $R_{2,\max}$: WLAN 1Gbit/s
- $R_{1,\max}$: MBWA Max 100Mbit/s
- $R_{1,\min}$: MBWA Min 1Mbit/s

$$F_{h3} = S\sqrt{R_{3,\max}\sqrt{R_{2,\max}\sqrt{R_{1,\max} \cdot R_{1,\min}}}} \quad (5)$$

- $R_{3,\max}$: WPAN 10Gbit/s

MBWA + WLAN + WPAN (10Gbit/s)

F = 4000

Research Area

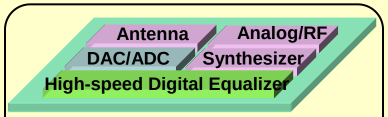
Hetero-Network Joint

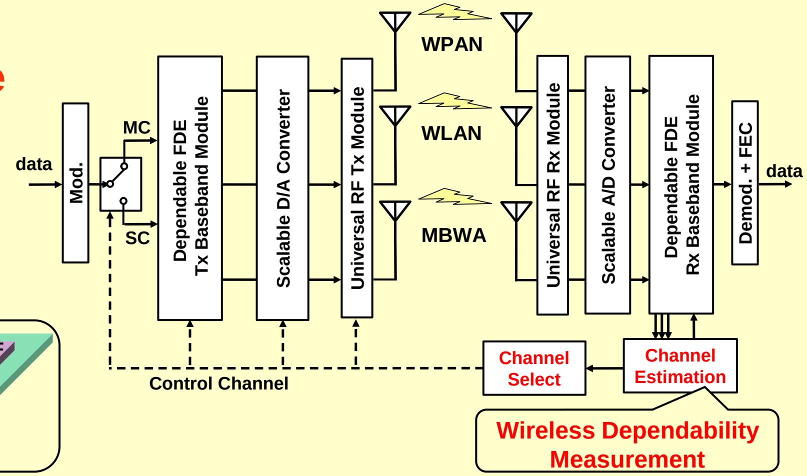
H2H, H2M, M2M

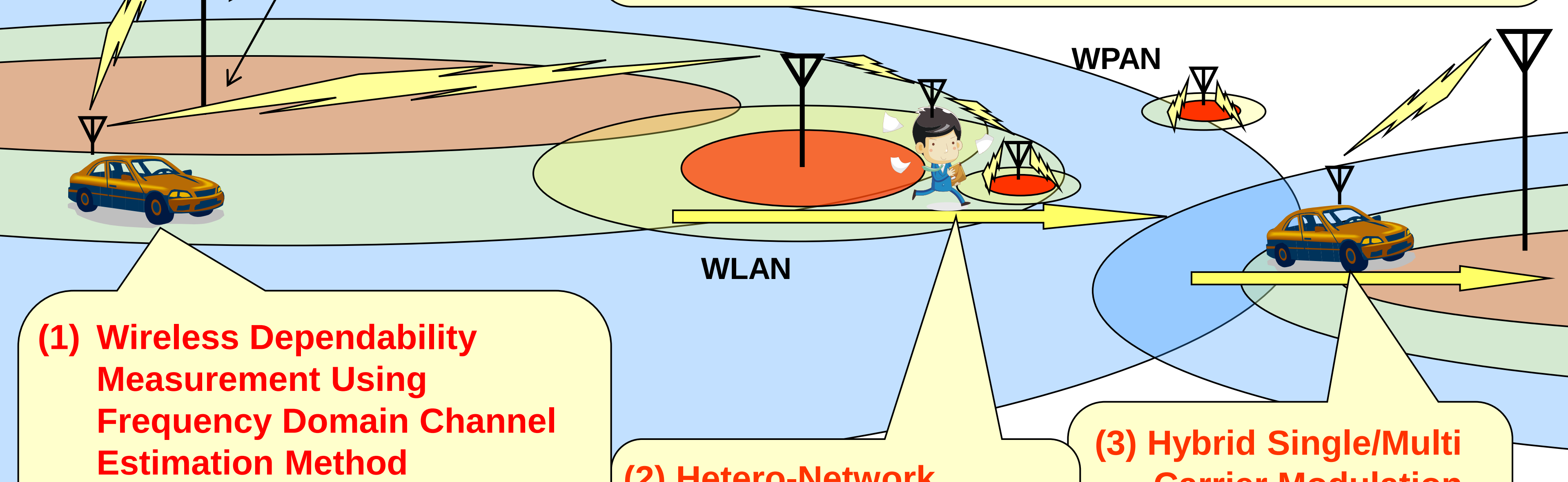
Information network & Control network

Dependable Air Interface

(1) Universal RF
(2) FDE
(3) Scalable A/D & D/A







(1) Wireless Dependability Measurement Using Frequency Domain Channel Estimation Method

+ Measuring multi channel functions simultaneously: distance, S/N, BER
+ Selection of optimum channels after channel compensation

(2) Hetero-Network System Handover

+ High mobility
+ Optimum channel selection

(3) Hybrid Single/Multi Carrier Modulation

+ Optimum modulation for distance, S/N, BER
+ Improving connectivity

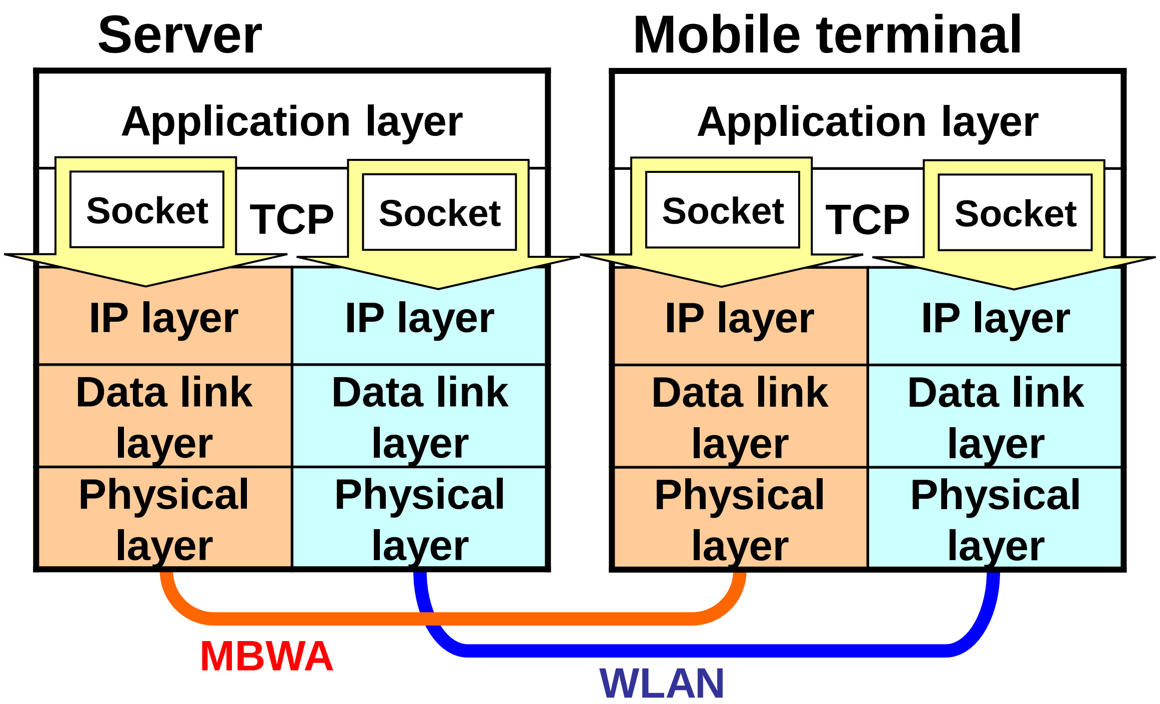
Seamless System Handover Method

[1] Japanese Patent #5049069

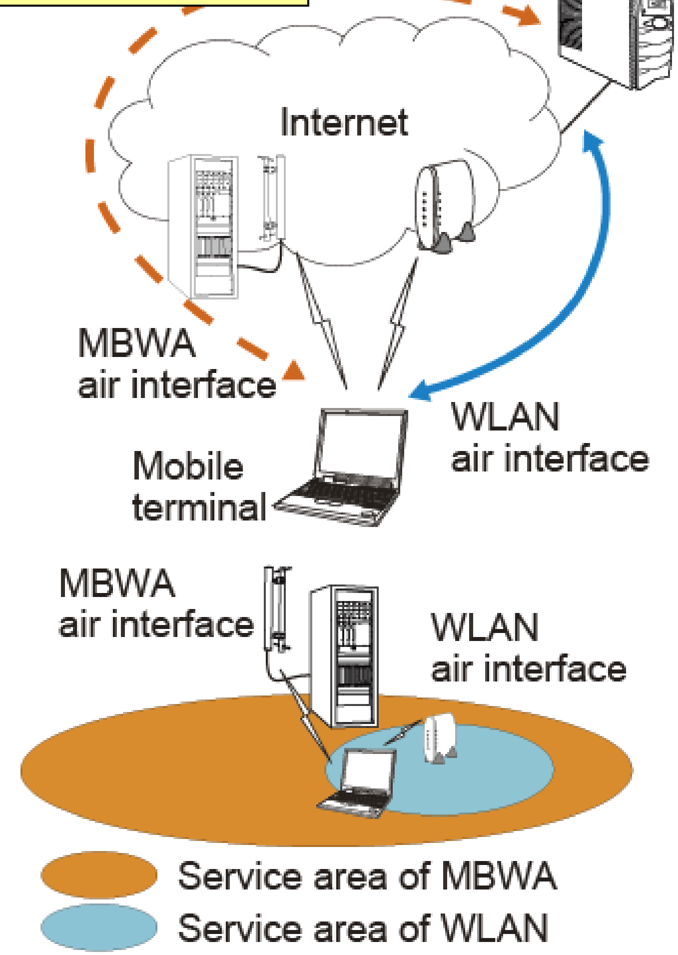
[2] S. Kameda et al., IEICE Trans. Commun., E95-B(4), 1152-1160, April 2012.

All handover functions are implemented in the application layer without requiring any upgrades of the infrastructures and terminals.

Protocol stack



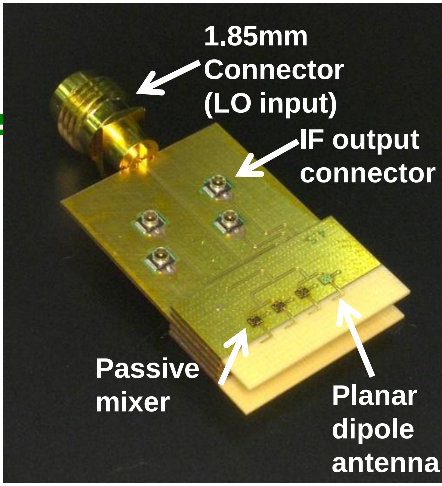
Network



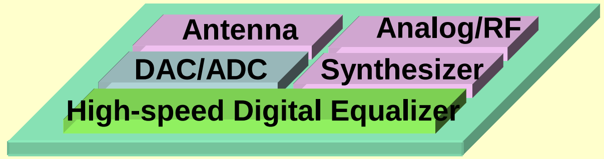
- **The developed programs use multiple sockets binding each air interface.**
- **The mobile terminal selects an air interface through selecting a socket to send/receive packets.**

Device Technology

Research Area



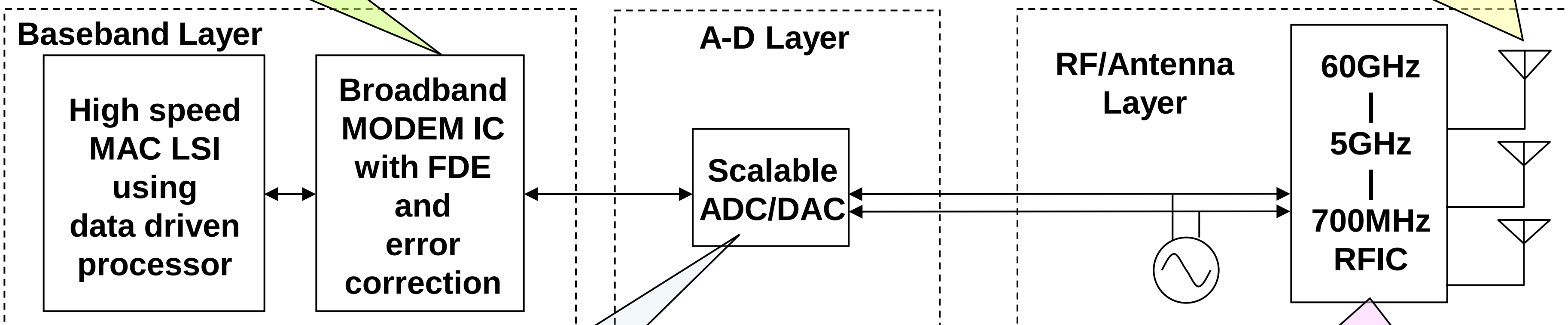
All Si-CMOS Broadband
SC/MC FFT/IFFT



Dependable Wireless System

2) Frequency Domain Equalization (FDE)

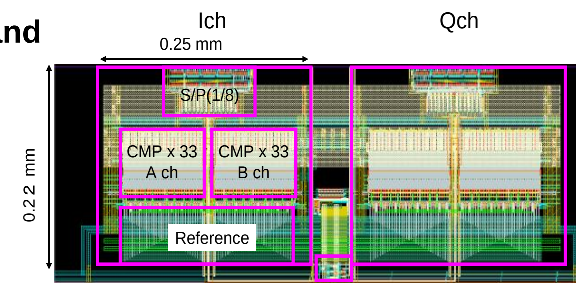
4) Antenna Module Using 3-D SiP Technology



3) Scalable ADC/DAC

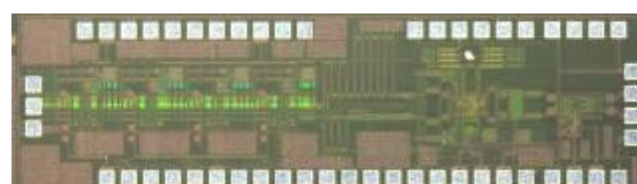
1) All Si CMOS RFIC（500MHz～70GHz）

■ **Flash ADC for 60GHz-Band Communication System**
5bit, 2.3GSps, 12mW



40nm CMOS

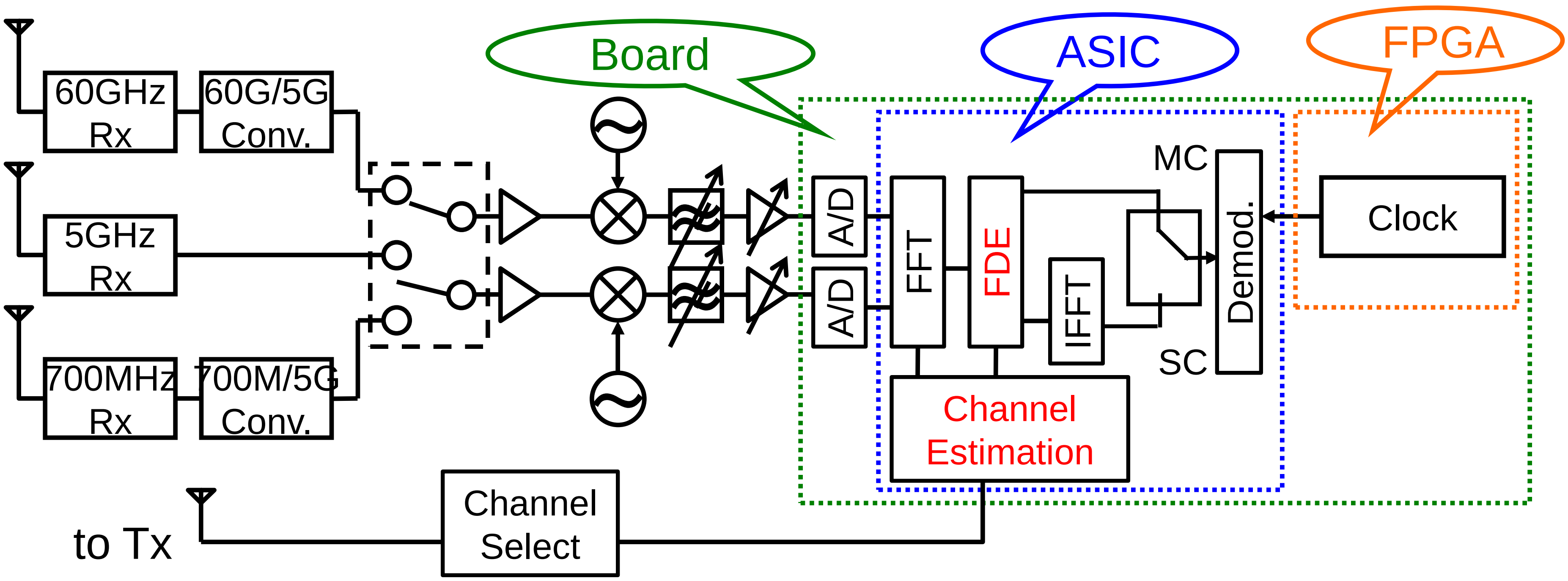
■ **60GHz-Band Receiver Front-End CMOS IC**
Chip size: 2.85mm×0.82mm



90nm CMOS

Realizing Scalable Frequency Domain Equalization for Heterogeneous Wireless System

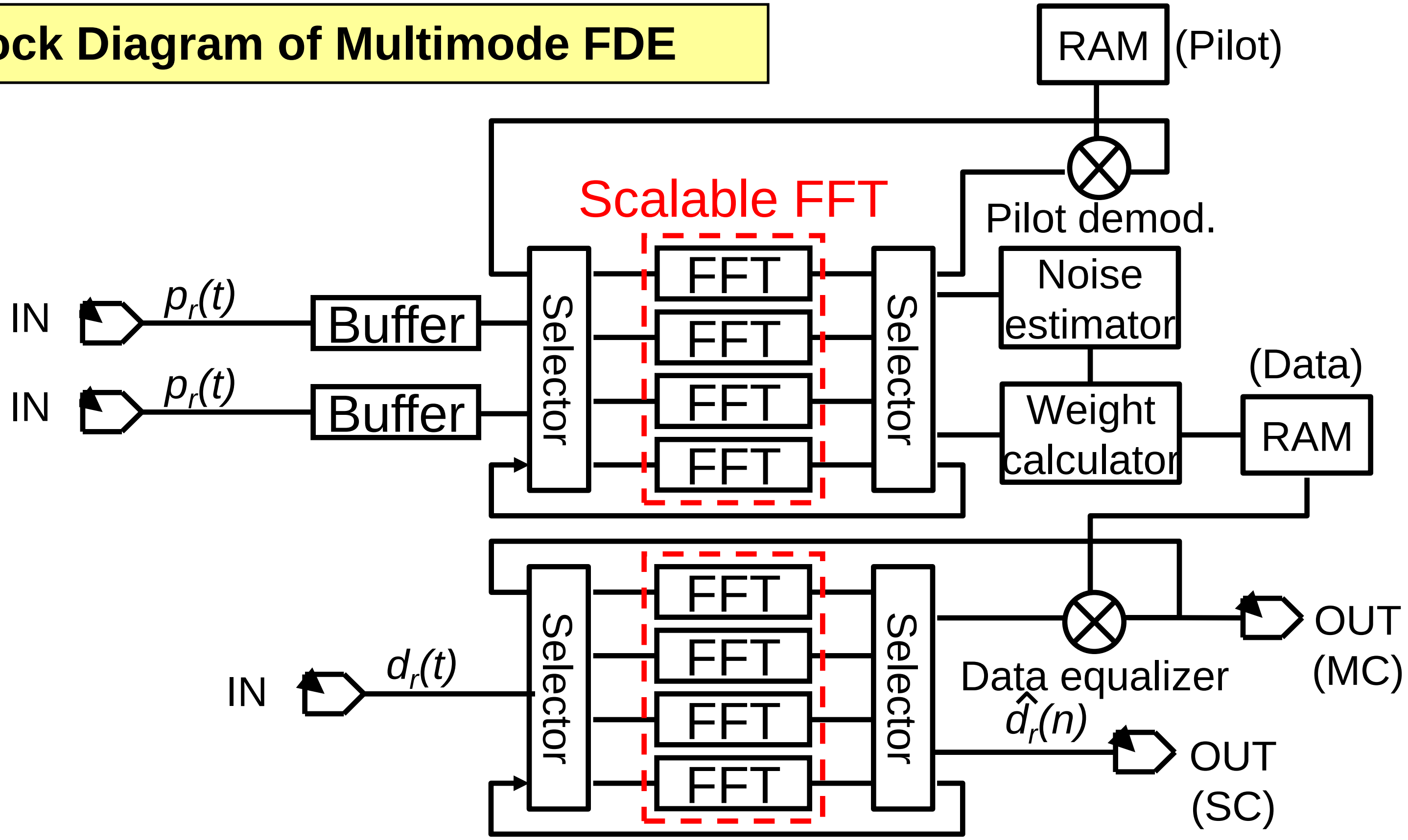
– ASIC Implementation of Baseband Circuit with Scalable FDE



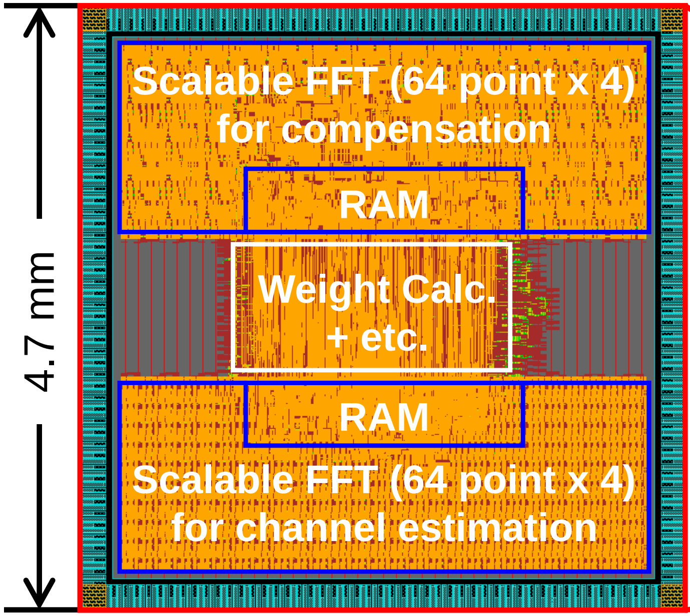
Multimode FDE Receiver: Design

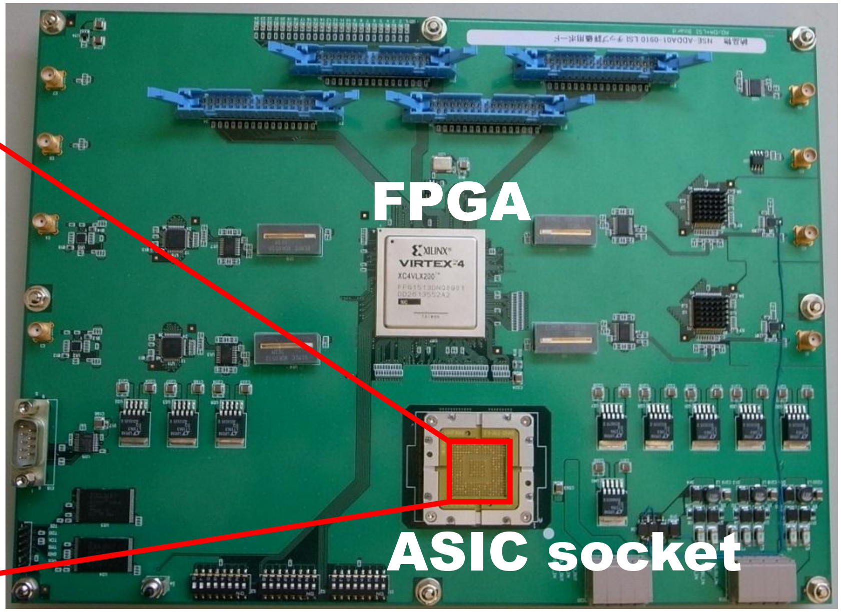
- Multimode: SC and/or MC signals
- Channel estimation: 2 channels simultaneously
- Two 256-point FFT/IFFT circuits (include 64 point x 4)
  - Each FFT is also able to work either two 128-point FFTs or four 64-point FFTs.
- Implemented estimation scheme: MMSE and ZF (zero forcing)

Block Diagram of Multimode FDE



Multimode FDE Receiver: ASIC implementation





ASIC specifications

Process	180nm CMOS
Total area (core area)	22.1 mm^2 (17.6 mm^2)
Throughput	48.1 Mbit/s at 100 Msample/s
Power consumption	660mW at 100 Msample/s

Evaluation board specifications

FPGA	Xilinx Corp. Virtex4 LX200
Clock frequency	100 MHz

CMOS: complementary metal-oxide semiconductor
FPGA: field-programmable gate array

Future Direction: Extended Dependable Air

Surface & Space Communications