

JST International Symposium on Dependable VLSI Systems 2012

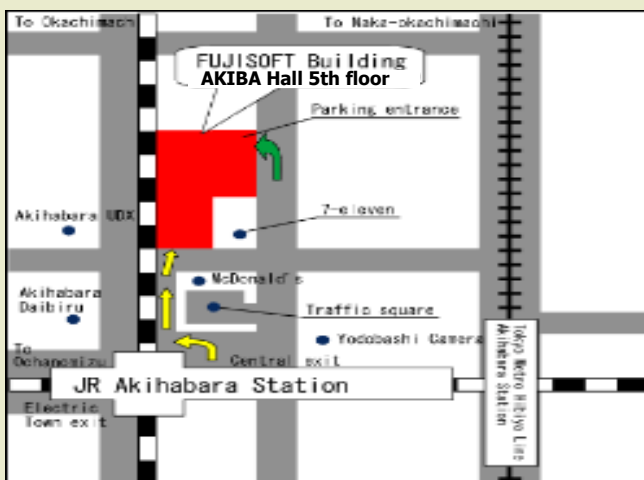
9:00-19:00 December 1st 2012
AKIBA Hall, Tokyo Japan

This is an announcement of the first JST International Symposium of Dependable VLSI Systems to be held in Tokyo on December 1st, 2012. The purpose of this symposium is to share the results of a research program entitled, "Dependable VLSI Systems" among professionals having special interest in dependability of micro-electronic systems around the world and promote cross-layer collaboration for dependable operation of systems.

This unique program, sponsored by JST (Japan Science and Technology Agency), was initiated in 2007 for establishing basic VLSI technologies to enhance the dependability of VLSI systems, which could range from automobile, plant, transportation, telecom, data processing to aerospace systems. The program currently has 11 projects running that address various issues, some arising from miniaturization on the one hand and complexity on the other, including five projects to be completed this fiscal year.

Symposium Highlights:

- 1)Sharing Grand Challenges for Dependable Systems from Different Aspects
Speakers: Sani Nassif (IBM), Subhasish Mitra (Stanford U), Koichiro Takayama (Fujitsu Lab.)
- 2)Exploring International Coordination with Foreign Projects
Speakers: Rajesh Gupta (UCSD), Joerg Henkel (Karlsruhe Institute of Tech.)
- 3)Presenting Research Achievements by 11 Teams of JST DVLSI Program
- 4)Discussing in Panel on Cross-Layer Optimization for Dependable Systems



Near Stations

1. Two minutes walk from Central exit of JR Akihabara Station
2. One minute walk from A3 exit of Tsukuba Express Station
3. Three minutes walk from No.2 exit of Tokyo Metro Hibiya Line Station

Address

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FUJISOFT Akihabara Bldg. 5th floor
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JST International Symposium on Dependable VLSI System 2012 (Tokyo, Dec. 1, 2012)

Program

9:00 Opening Remarks from Shojiro Asai (Chair: H. Onodera)

9:20 Session 1. Dependability Challenges (Chair: Y. Matsunaga)

Dependability Challenges at the Device and Circuit Level

Sani Nassif, IBM

Robust System Design: Overcoming Complexity and Reliability Challenges

Subhasish Mitra, Stanford Univ.

Challenges to develop highly reliable HPC systems

Koichiro Takayama, Fujitsu Lab.

10:50 Break

11:10 Session 2. Dependability Research around the World (Chair: H. Onodera)

The Variability Expeditions: Exploring the Software Stack for Underdesigned Computing Machines

Rajesh Gupta, Univ. California, San Diego

Dependable Embedded Systems – The SPP 1500 Research Program

Joerg Henkel, Karlsruhe Institute of Tech.

12:10 Lunch

13:30 CREST DVLSI presentations (Chair: S. Kameda)

H. Onodera, M. Fujita, K. Tsubouchi, H. Yasuura, M. Koyanagi

S. Kajihara, M. Yoshimoto, T. Yoneda, K. Takeuchi, T. Fujino, N. Yamasaki

15:00 CREST DVLSI Posters

16:00 Panel Discussion (Moderator: M. Hashimoto)

Toward Cross-Layer Optimization for Dependable Systems

Panelists: Dan Alexandrescu (iRoC Technologies), Bhargab Bikram

Bhattacharya (Indian Statistical Institute), Bartek Gedrojc (Riscure), Ken

Takeuchi (Chuo Univ.), Hoi-Jun Yoo (KAIST)

Commentators: Rajesh Gupta (UCSD), Joerg Henkel (Karlsruhe Institute of

Tech.), Subhasish Mitra (Stanford Univ.), Sani Nassif (IBM), Koichiro Takayama

(Fujitsu Lab.), Jinyun Zhang (Mitsubishi Electric Research Lab.)

17:20 Closing Remarks

17:30 Banquet (-19:00)

Registration

Invited attendees: Invitation will be extended to solicit attendance.

General registration: welcome to pre-register at <http://www.dvlsi.jst.go.jp/english/index.html>

Registration Fee: free for all sessions, and 4,000 JPY for banquet

Contact: symposium secretariat (dvlsi@dvlsi.jst.go.jp)



[JST/CREST Program 'Dependable VLSI Systems'](http://www.dvlsi.jst.go.jp/english/index.html)

<http://www.dvlsi.jst.go.jp/english/index.html>

Program Committees

Chair:	Hidetoshi Onodera	(Kyoto University)
Secretary:	Masanori Hashimoto	(Osaka University)
Members:	Mitsumasa Koyanagi	(Tohoku University)
	Masahiro Goshima	(University of Tokyo)
	Suguru Kameda	(Tohoku University)
	Hiroshi Oguma	(Toyama National College of Technology)
	Yusuke Matsunaga	(Kyushu University)

Research Supervisor

Shojiro Asai (Vice President, Rigaku Corporation)

Research Area Advisers

Masatoshi Ishikawa	(Professor, The University of Tokyo)
Tohru Kikuno	(Professor, Osaka Gakuin University)
Tadayuki Takahashi	(Professor, Japan Aerospace Exploration Agency)
Naoki Nishi	(General Manager, NEC Corp., System IP Core Research Lab.)
Atsushi Hasegawa	(Director, Renesas Electronics Corp.)
Toshio Masubuchi	(Director, Toshiba Corp. Semiconductor & Storage Company)
Kazuo Yano	(Senior Chief Researcher, Hitachi Ltd. Central Research Lab.)
Koichiro Takayama	(Chief Researcher, Fujitsu Laboratory Ltd.)

Principal Investigators and Research Themes

1. Hidetoshi Onodera (Kyoto University) URL <http://www.tamaru.kuee.kyoto-u.ac.jp/>
“Dependable VLSI platform using robust fabrics”
2. Shuichi Sakai (The University of Tokyo) URL <http://www.mtl.t.u-tokyo.ac.jp/index-e.html>
“Ultra Depedable VLSI by collaboration of formal verifications and architectural technologies”
3. Kazuo Tsubouchi (Tohoku University) URL <http://www.riec.tohoku.ac.jp/lab/it-21-mob/index-e.html>
“Development of Dependable Wireless System and Device”
4. Hiroto Yasuura (Kyushu University) URL http://dvlsi.c.csce.kyushu-u.ac.jp/index_e.html
“Modeling, Detection, Correction and Recovery Techniques for Unified Dependable Design”
5. Seiji Kajihara (The Kyushu Institute of Technology) URL <http://aries3a.cse.kyutech.ac.jp/>
“Circuit and system mechanisms for high field reliability”
6. Masahiko Yoshimoto (Kobe University) URL <http://www28.cs.kobe-u.ac.jp/en/>
“Dependable SRAM Techniques for Highly Reliable VLSI System”
7. Tomohiro Yoneda (National Institute of Informatics) URL http://www.nii.ac.jp/staff/Yoneda_Tomohiro.shtml
“Development of Dependable Network-on-Chip Platform”
8. Mitsumasa Koyanagi (Tohoku University) URL <http://www.sd.mech.tohoku.ac.jp/Site/Home.html>
“Three-Dimensional VLSI System with Self-Restoration Function”
9. Ken Takeuchi (Chuo University) URL http://www.takeuchi-lab.org/index_e.htm
“Dependable Wireless Solid-State Drive (SSD)”
10. Takeshi Fujino (Ritsumeikan University) URL <http://www.ritsumeikan.ac.jp/se/re/fujinolab/index-e.html>
“The Design and Evaluation Methodology of Dependable VLSI for Tamper Resistance”
11. Nobuyuki Yamasaki (Keio University) URL <http://www.ny.ics.keio.ac.jp/>
“Fundamental Technology on Dependable SoC and SiP for Embedded Real-Time Systems”

